Advance VLSI Chip Design (Module 24513) Phase5

Munawar Ali

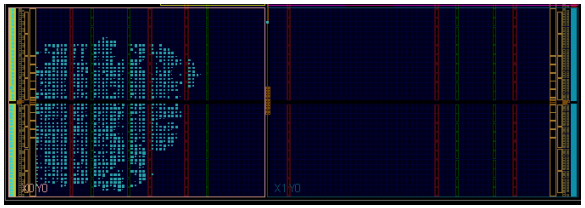
Aim of the Phase5

Creating Chip Layout for the Filter Design Using Cadence Innovus

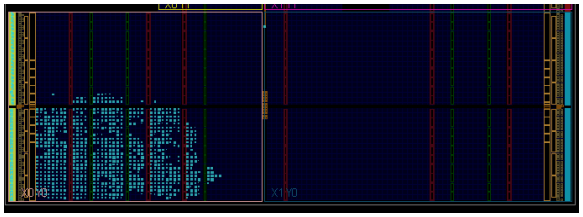
Design Optimization Flow

1)

2)



3)



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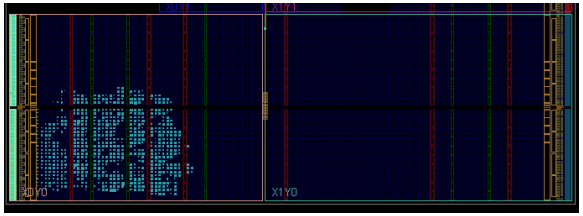

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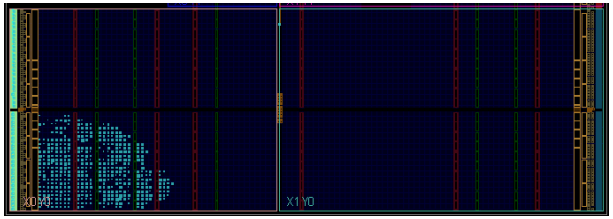

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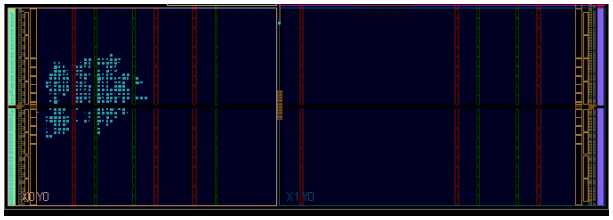

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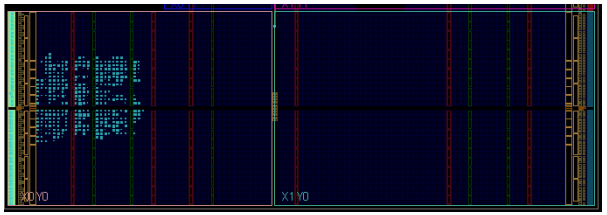
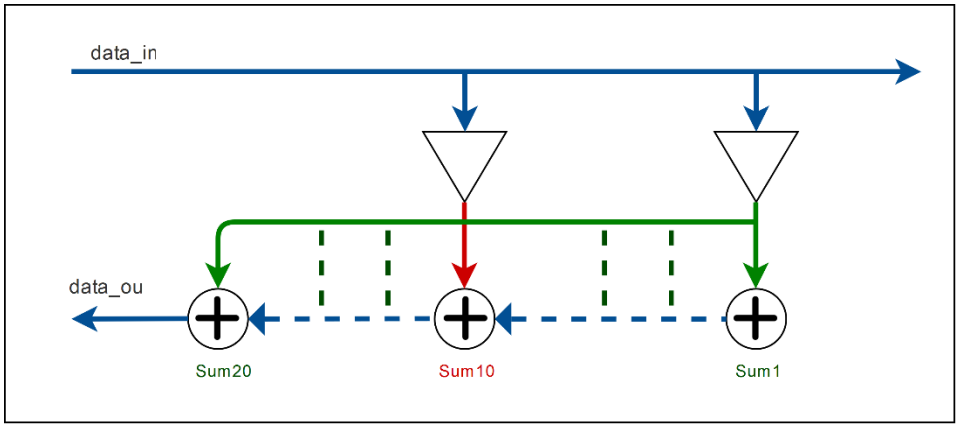


Design and Architecture

Final Filter Design

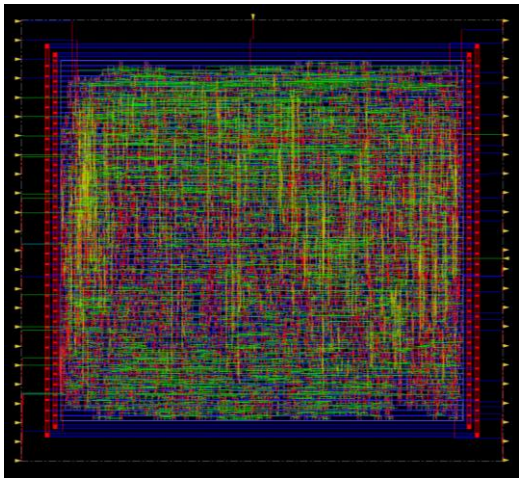
- 24-bit Carry Select Adder (used 20 times)
- Two Specific CSD multipliers



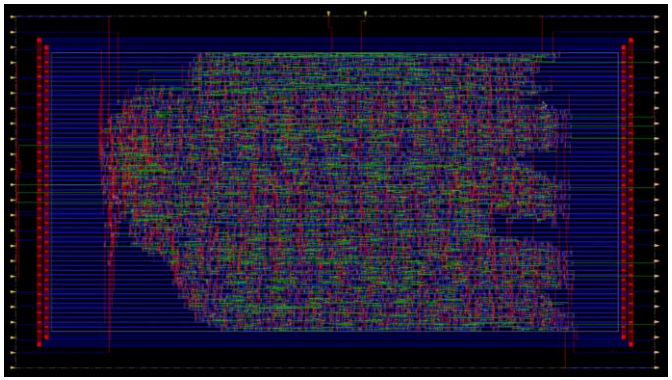
	Speed	Area	Voltage	Pow(dym)	Pow(leak)
1	1GHz	18999.9	1.1V	20.88mW	15.33uW

Cadence Parameters

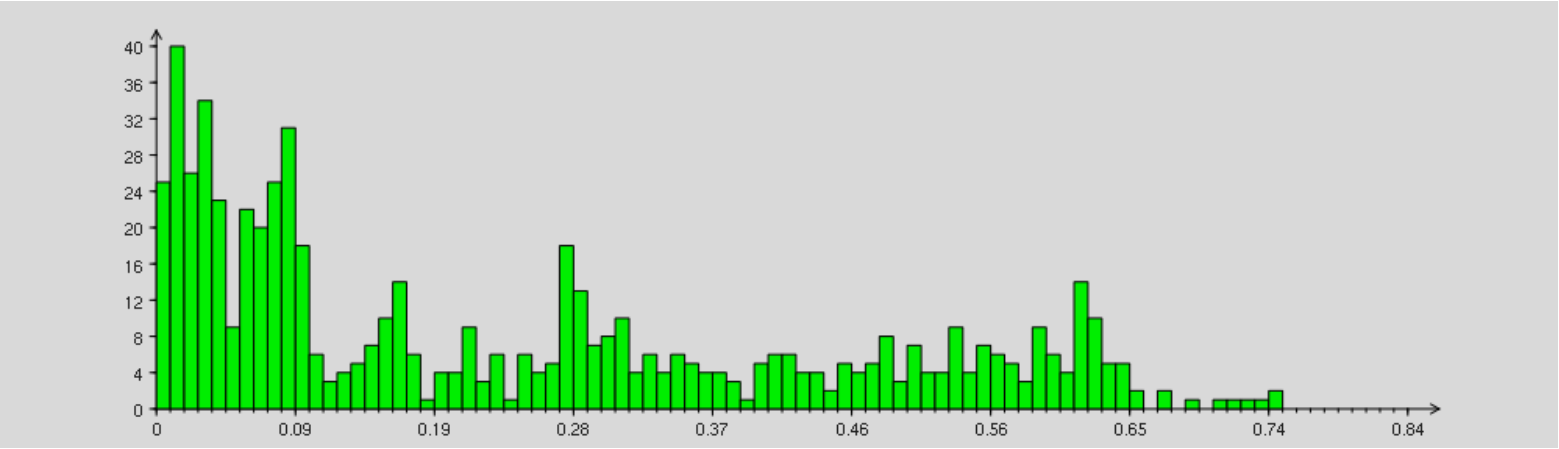
Core Utilization	75%
Aspect Ratio H/W	~0.80
Slack	~ -0.3



Core Utilization	40%
Aspect Ratio H/W	0.5
Slack	0.008



Filter Slack Histogram



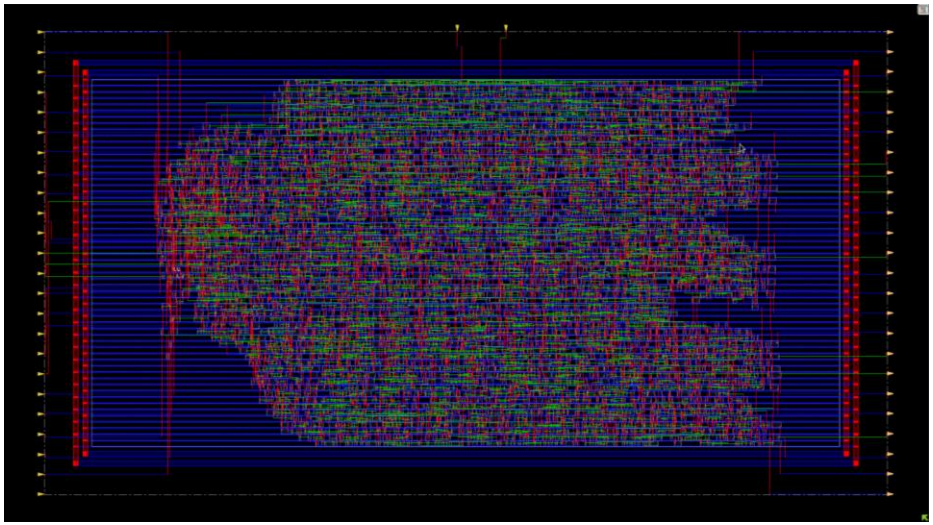
Comparison of all Designs

	#LUT	#FF	Slack ns
FPGA	9650	528	*-24.130*
	3411	1528	2.107
	2816	1486	1.075
	2274	1505	2.638
	1521	932	3.484
	727	632	2.814
	1107	663	3.262

	Freq	Voltage	Pow_{dy}	Pow_{leak}
ASIC	1 GHz	1.3 V	80 mW	30 uW
	1.1GHz	1.3 V	60 mW	25 uW
	1 GHz	1.2 V	50 mW	22 uW
	1 GHz	1.2 V	25 mW	20.2 uW
	1 GHz	1.1 V	20 mW	15.3 uW
	1 GHz	1.1 V	20.9 mW	15.3 uW
	1 GHz	1.1 V	21.82 mW	15.33 uW

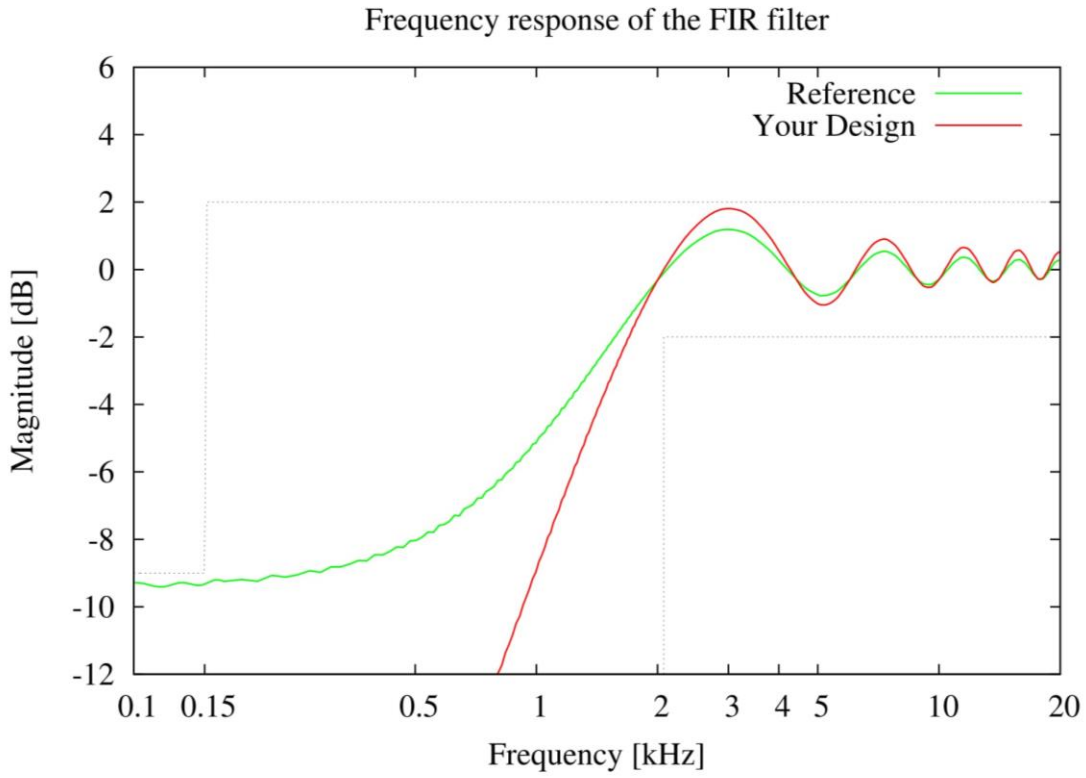
Final Layout Parameters

Frequeny	1 GHz
Attenuation	28.624749
# Total Pipelines	4
Chip Size	68000.407 um^2
Core Size	47800.207 um^2
Core Utilization	39.88%
Pow(dyn)	21.8235 mW
Pow(leak)	15.33905 uW
Metric	8.55 x exp7



Result

Final Frequency Response



THANK YOU

Questions!