Advance VLSI Design (Module 24151) Phase 5

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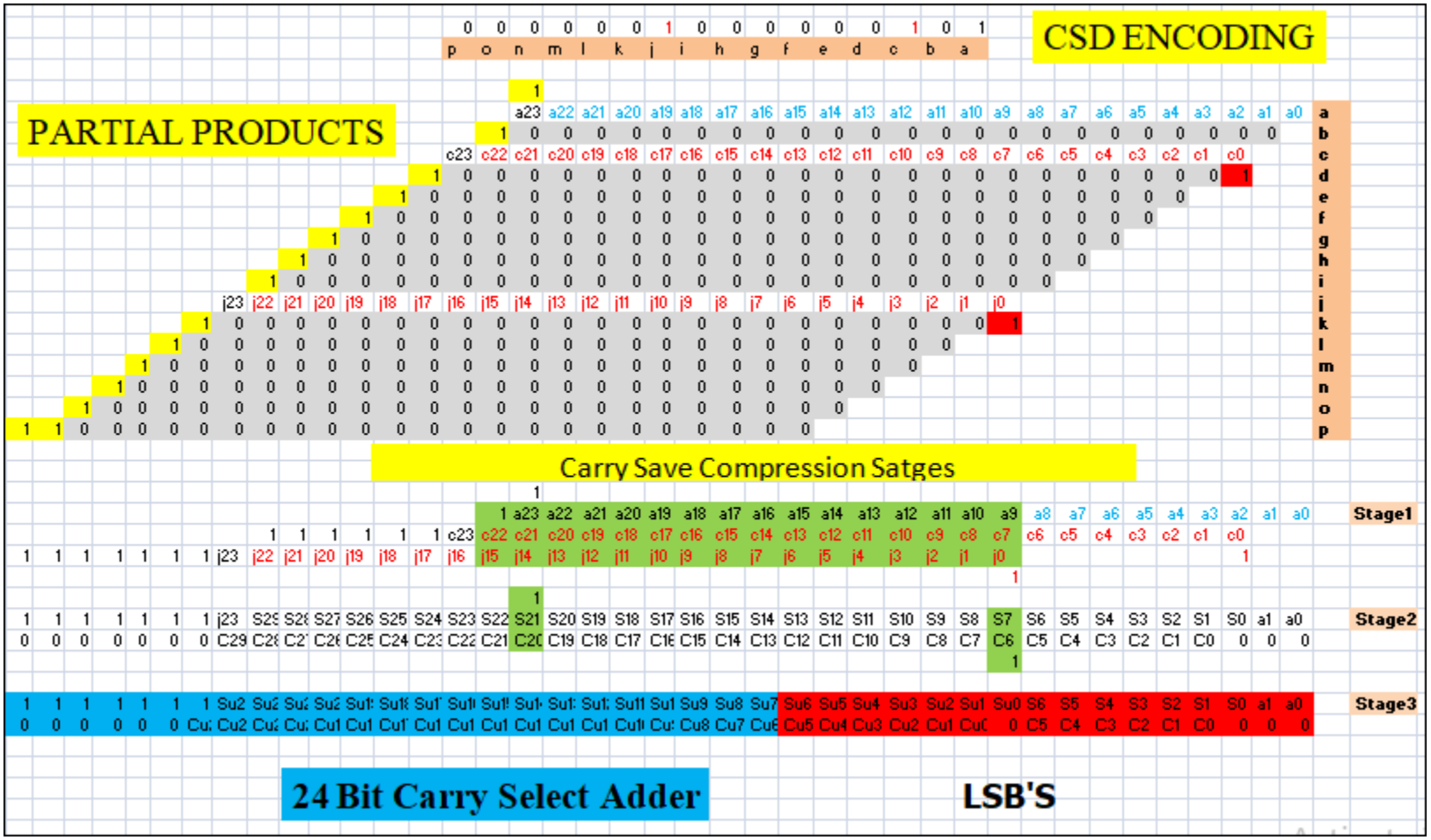
Aim of Phase 5 Task

Complete ST65 layout and backannotated Results

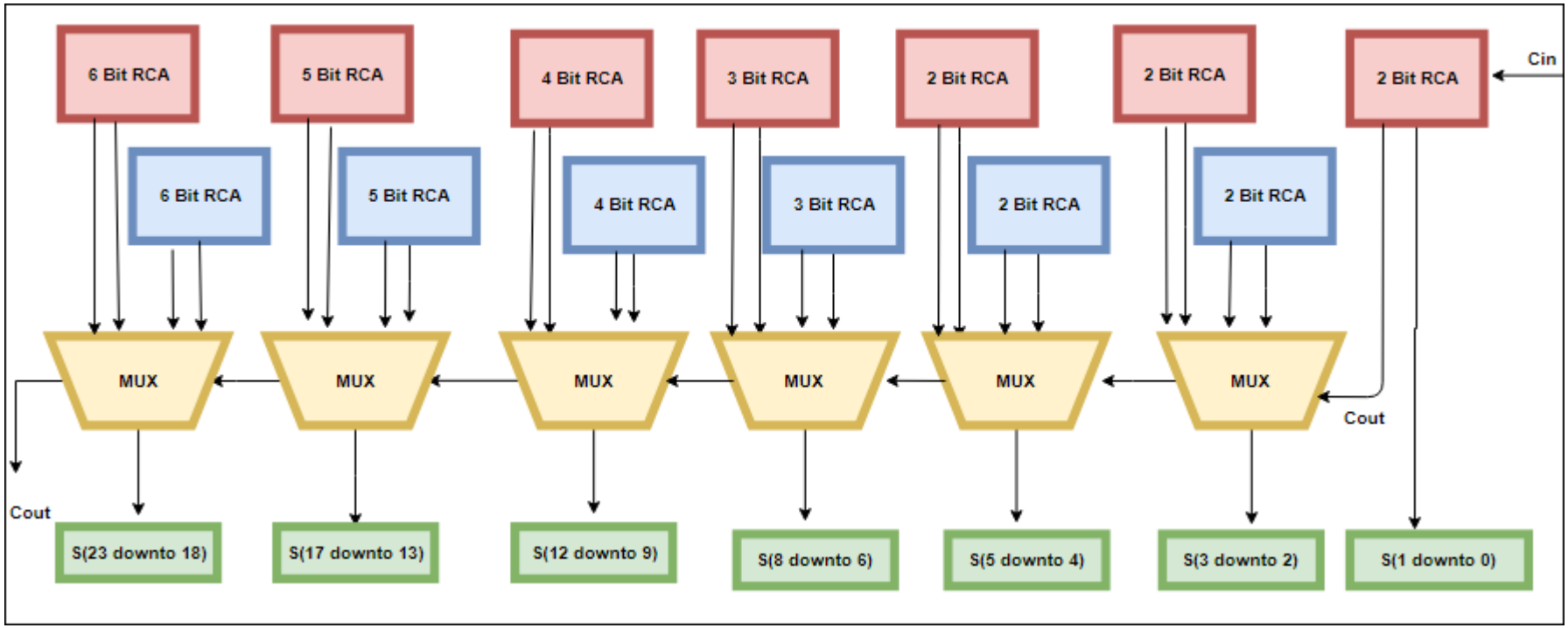
Design and Architecture

- CSD Encoded Wallace Tree Multiplier
- Variable Group Size Carry Select Adder

CSD Encoded Wallace Tree Multiplier

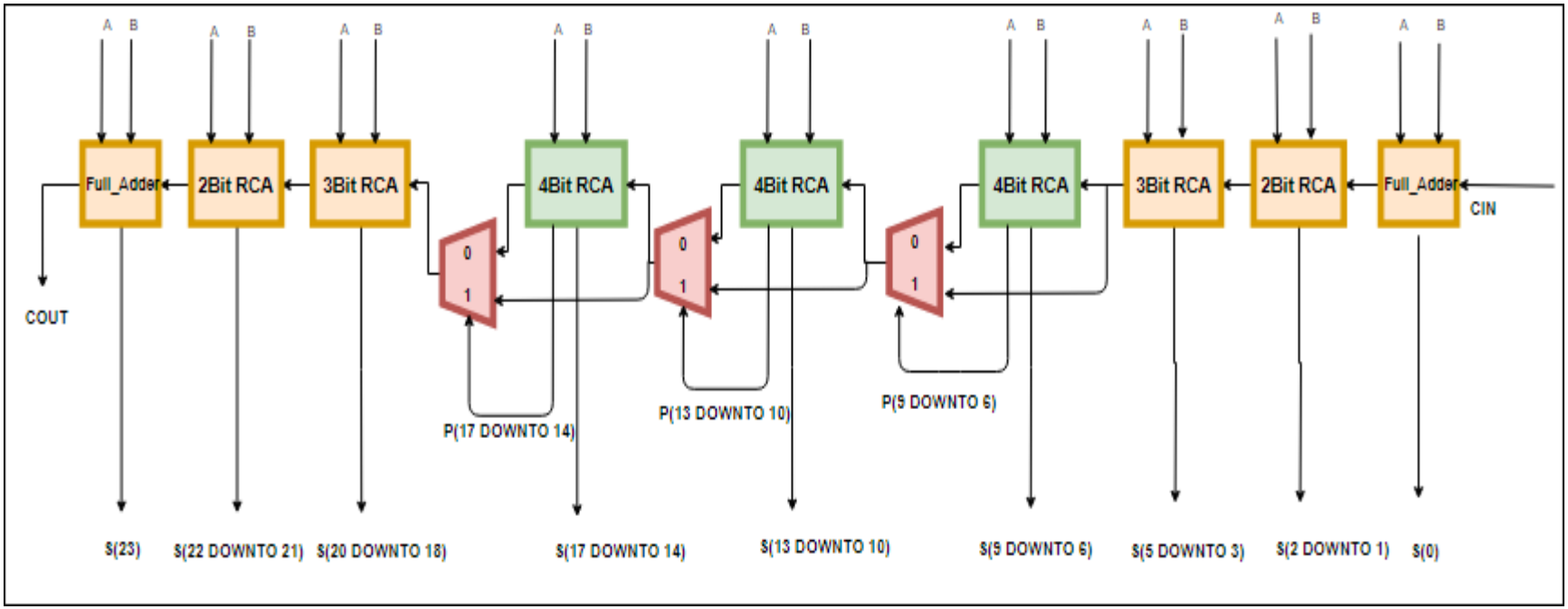


24 Bit Carry Select Adder



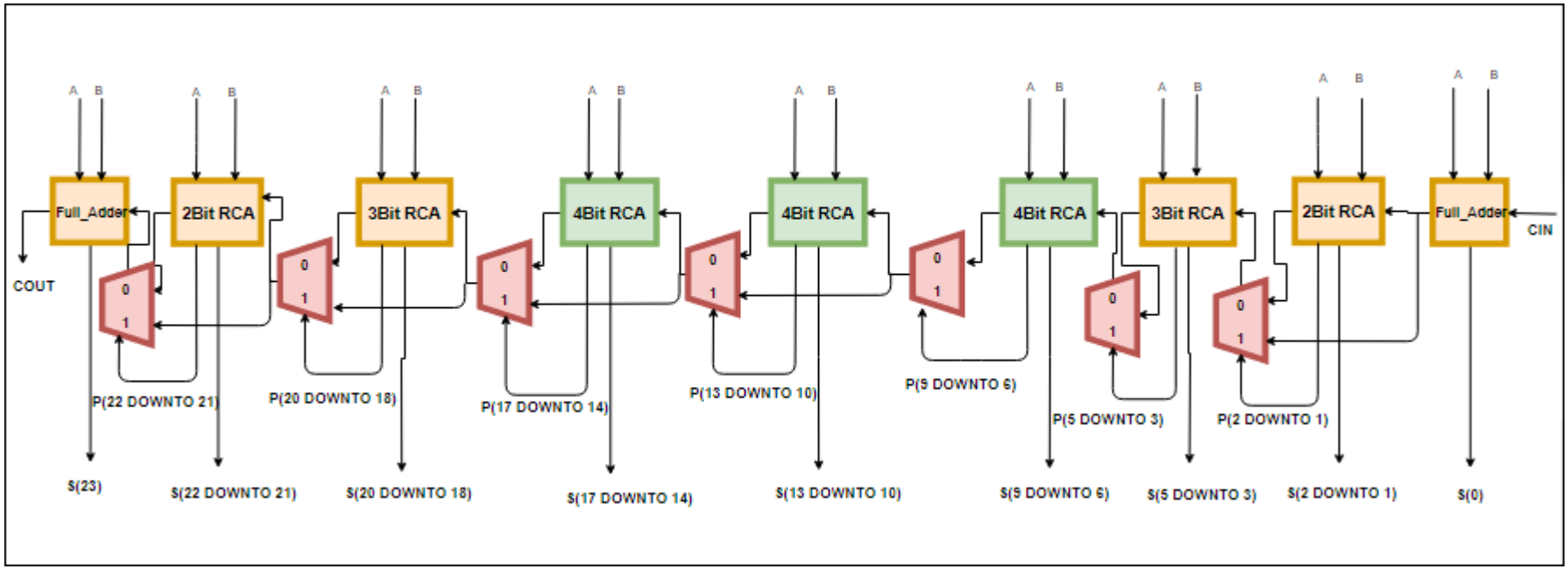
Issues

Carry Skip Adder



Frequency:799MHz

Modified Carry Skip Adder



Frequency: 799MHz

Cadence Tool Issues

•Design was achieving 1GHz by using all libraries.

•Core Utilization 65%,75% Negative Slack even after design optimization by using ECO.

•Core Utilization 50%,60% Positive slack after two times optimization of Design.

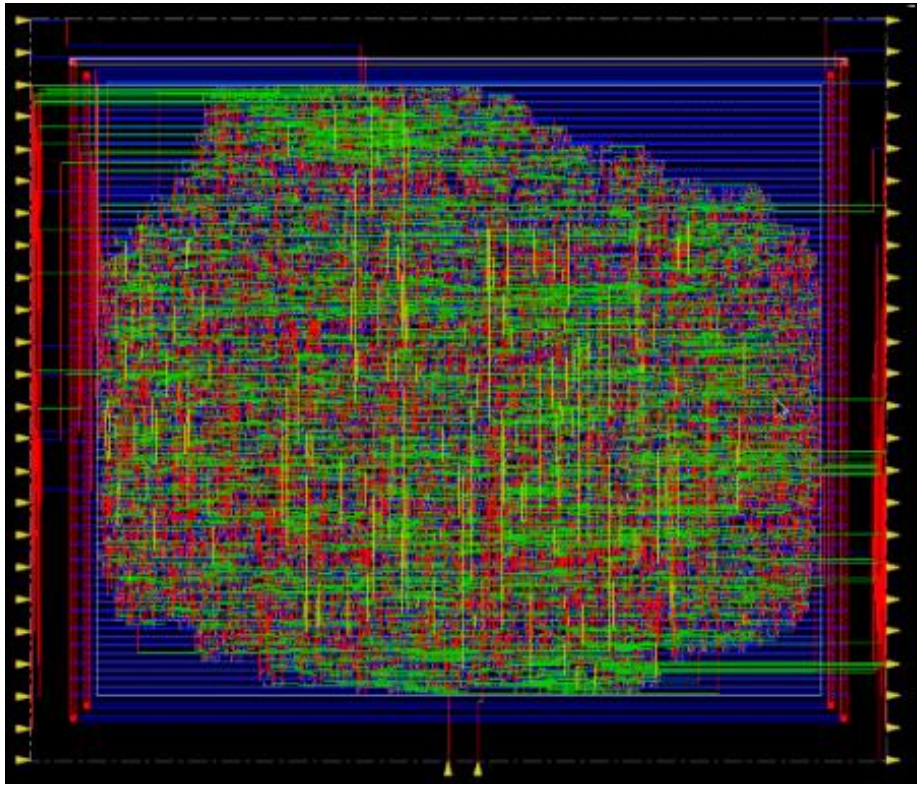
•When Timing Driven routing is used it was giving Positive slack on only one time optimization of Design.

Final Parameters of Cadence Tool

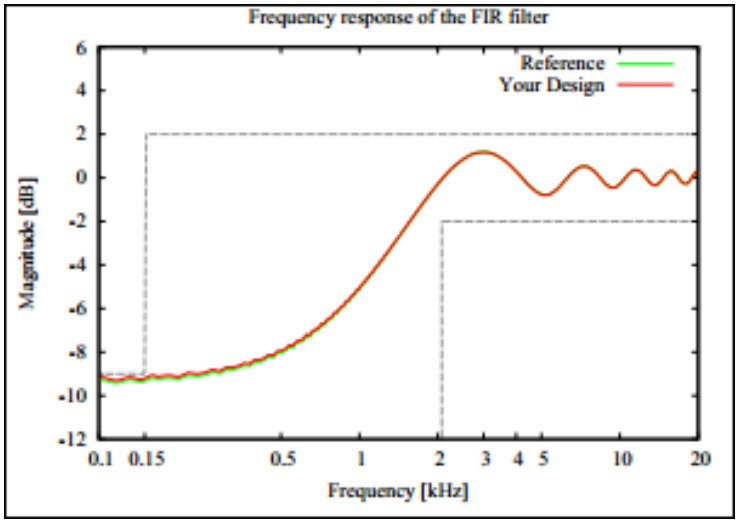
- **CORE65LPSVT,CORE65LPHVT,CORE65LPLVT**
- **Multi-Mode Multi Corner Configuration**(Voltage 1.2)
- **Floor Planing**:Core Utilization(50%)
- **Placement**: No of CPUs: 8
- **Power Planing**:Nets(VDD,GND)
- **Routing**:Nano route(Fix Antenna,Timing Driven)
- **ECO**: Design Optimization (Post route: Max Fanout)

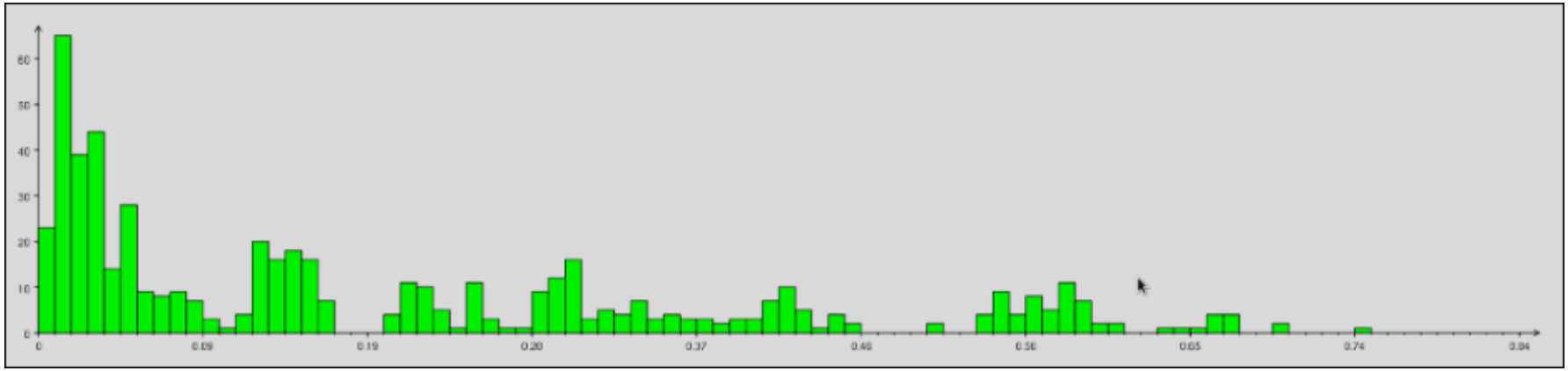
Design Parameters & Chip Layout

Frequency	**1000MHz**
Dynamic Power	**28.4232mW**
Leakage Power	**23.8899uW**
# Pipeline Satges	**2**
Metric	**-13.345 x10^6**
Core Size	**41601.456um^2**
Core Utilization	**50.598%**



Path Histogram & Frequency Response





THANK YOU

QUESTIONS?