Selected Topics in VLSI Design (Module 24513)

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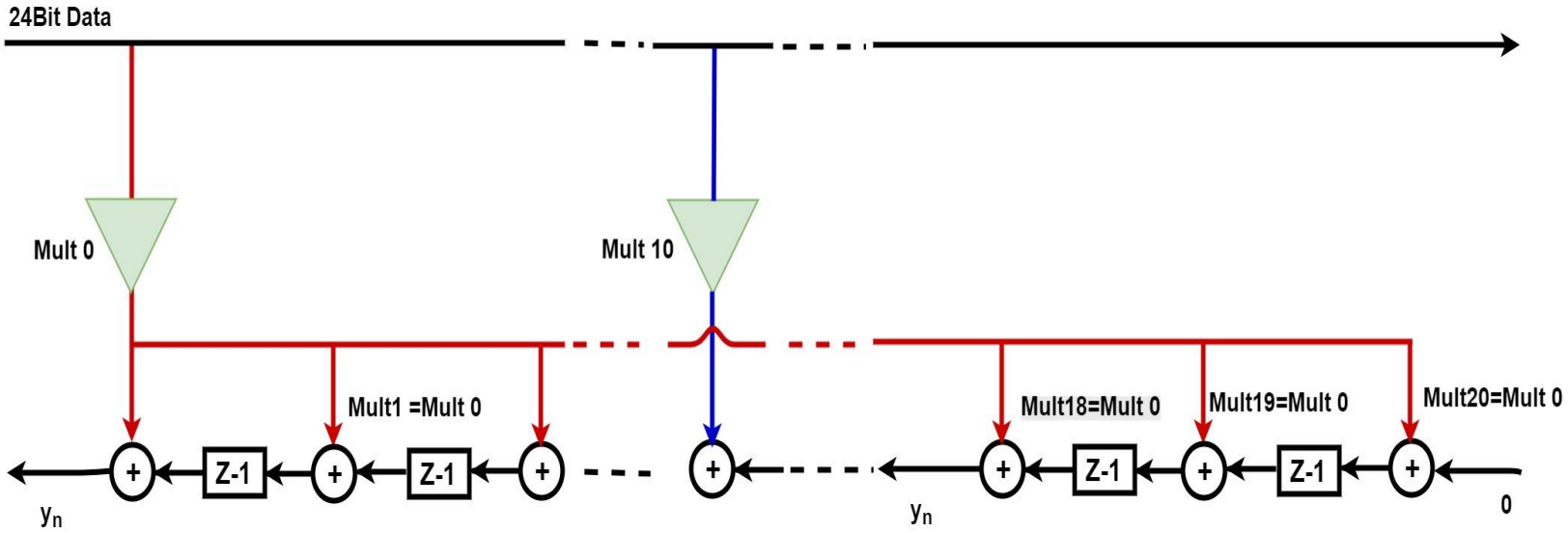
Aim of Task 5

Presentation of complete chip layout and its results

Implemented Design

- 18 bit Carry select Adder
- 18 bit multiplier
- Coefficient reduced from 21 to 2
- Achieve 1Ghz Frequency



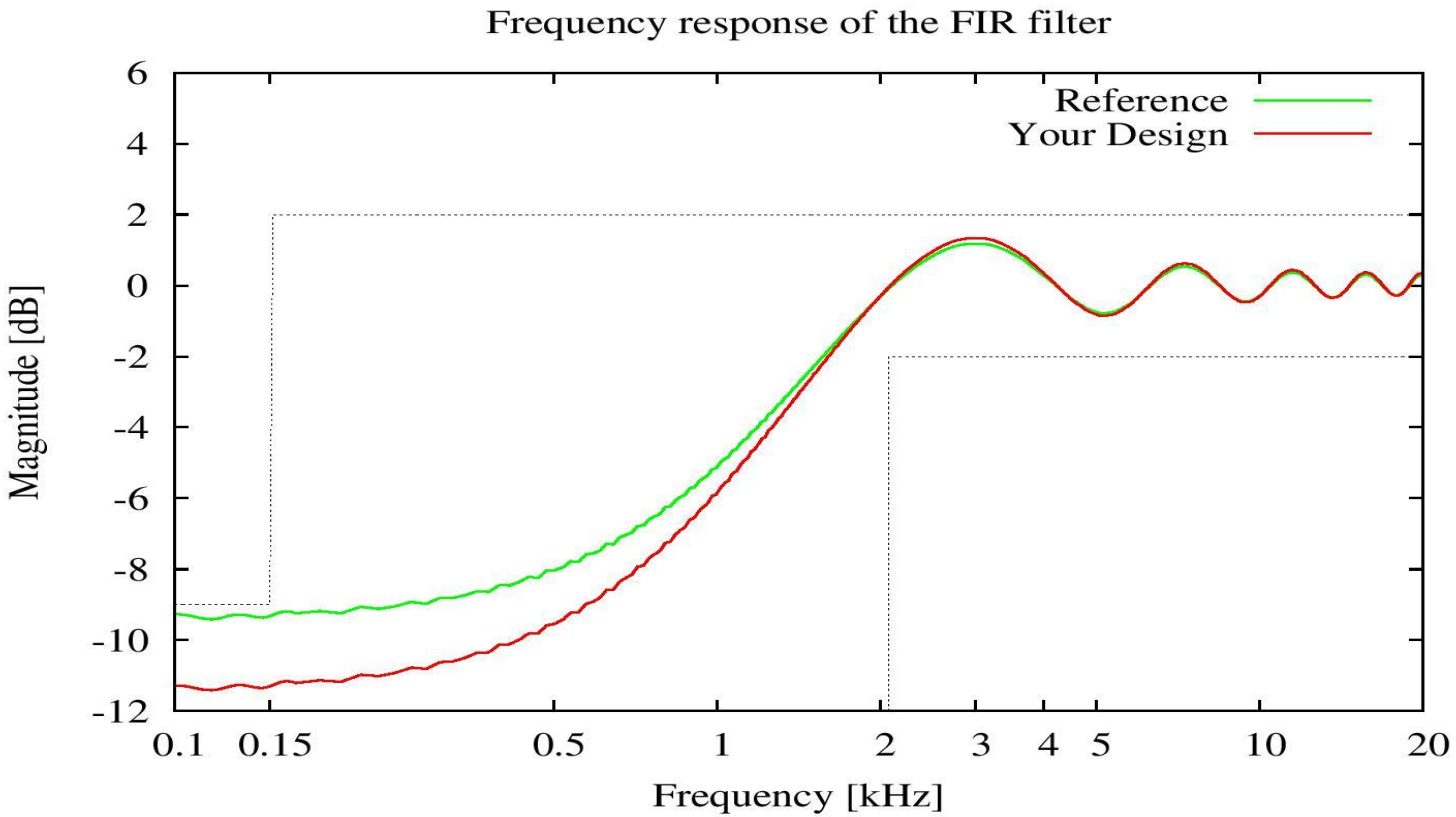
Observations

	Attenuation	Dynamic power	Leakage Power	Cell Area	Voltage	Metric
Task 4 Result	-9.07	32.4 mW	29.5µW	24564	1.2v	9.47*10^6
change coefficients	-9.23	30.92mW	27.60µW	23126	1.2v	1.07*10^7
New coefficients	-11.14	41.34mW	3.01µW	25716	1.3v	8.93*10^7
By using library	-11.14	35.39mW	30.22µW	24624	1.2v	1.04*10^7
By reducing adder & multiplier 18bit	-11.14	27.75mW	2.07µW	17544	1.3v	1.93*10^8

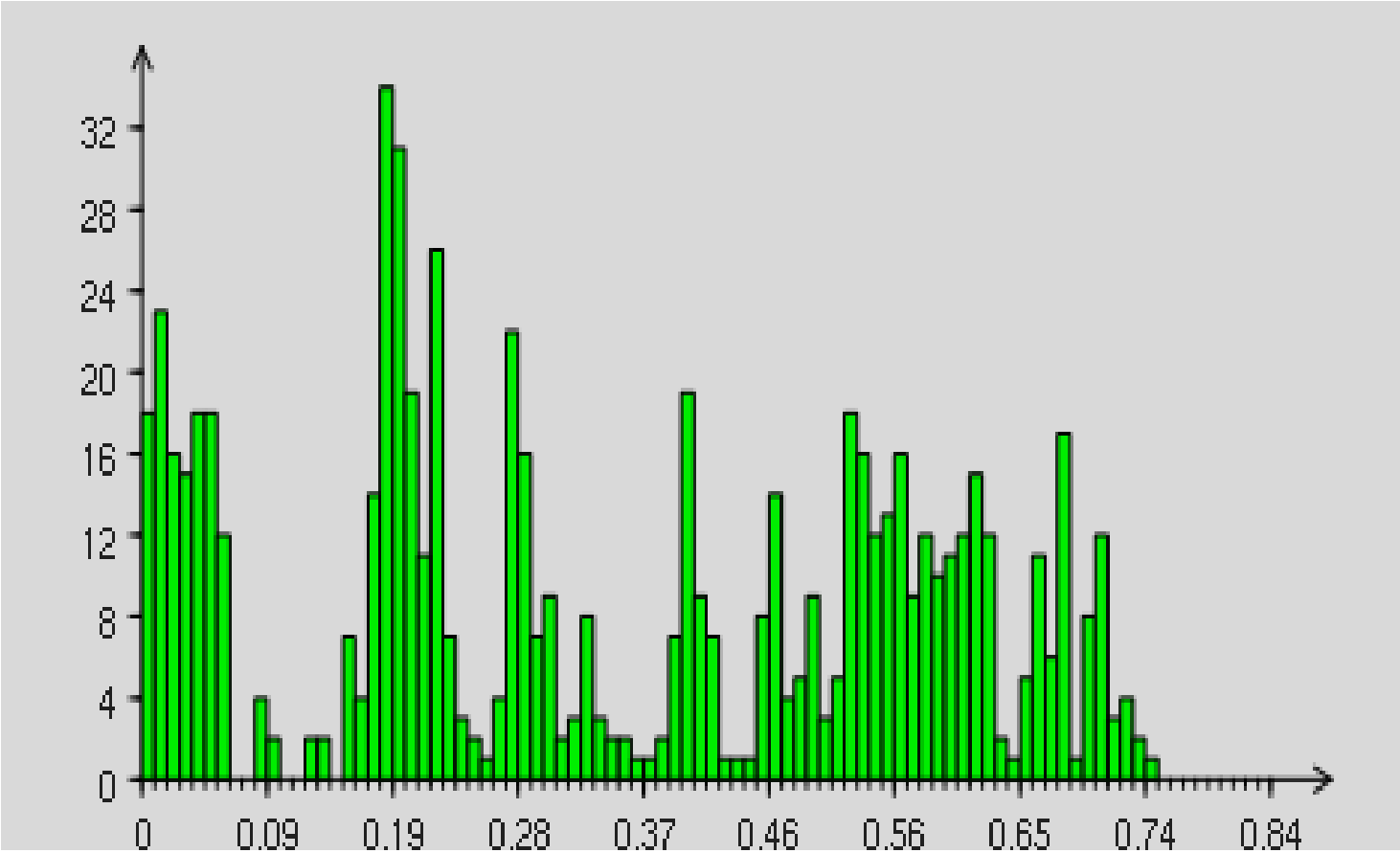
Final Results

Dynamic power	27.75mW
Leakage Power	2.07µW
Pipeline Stages	4
Attenuation	-11.14
Core size	23392.655 µm²
Core utilization	75.11 %
Metric	1.93*10^8

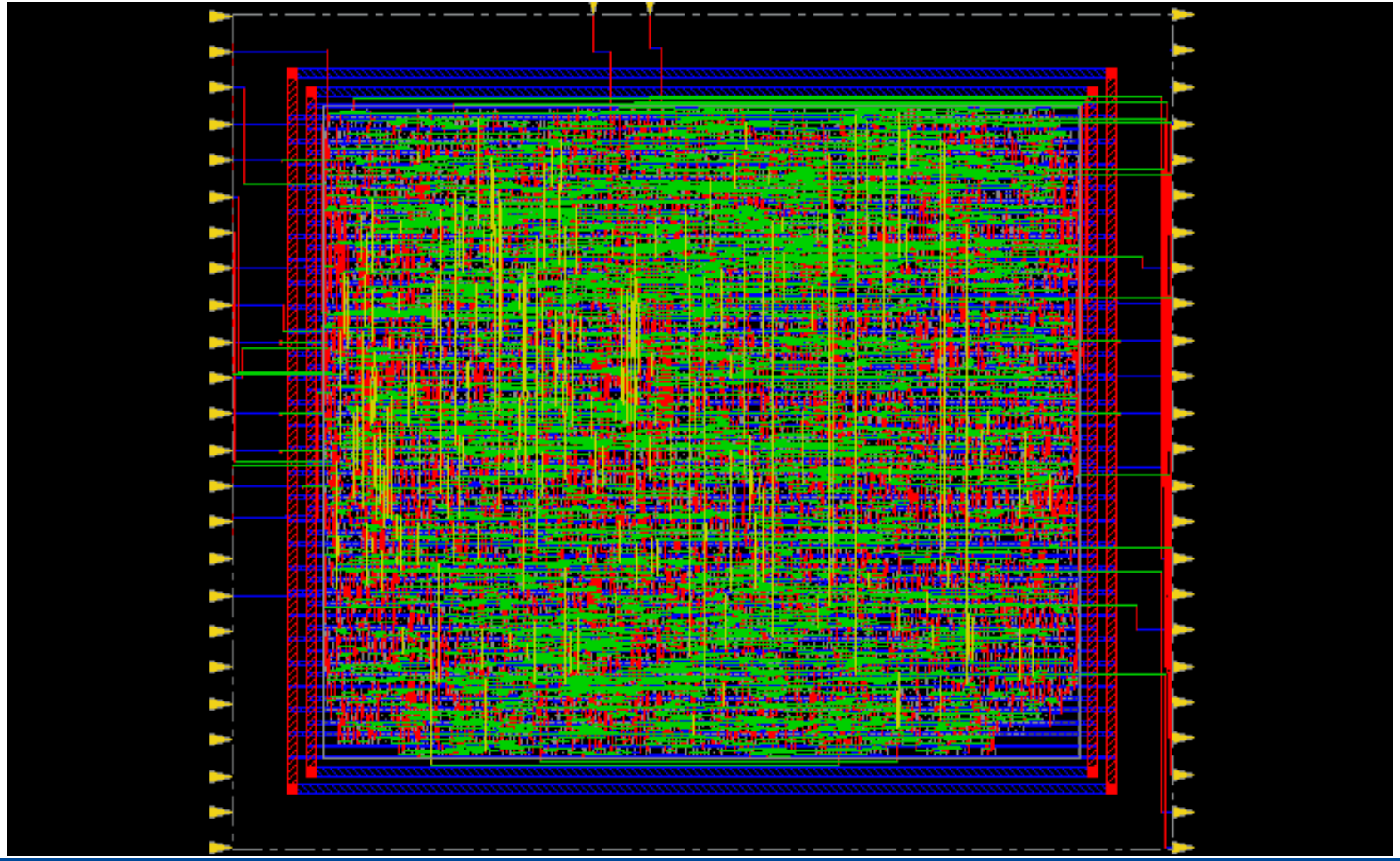
Frequency Response



Path histogram



Chip layout



THANK YOU