Universität Rostock Traditio et Innovatio

Institut für Angewandte Mikroelektronik und Datentechnik

Advanced VLSI (Project)

Module (24513)

By:
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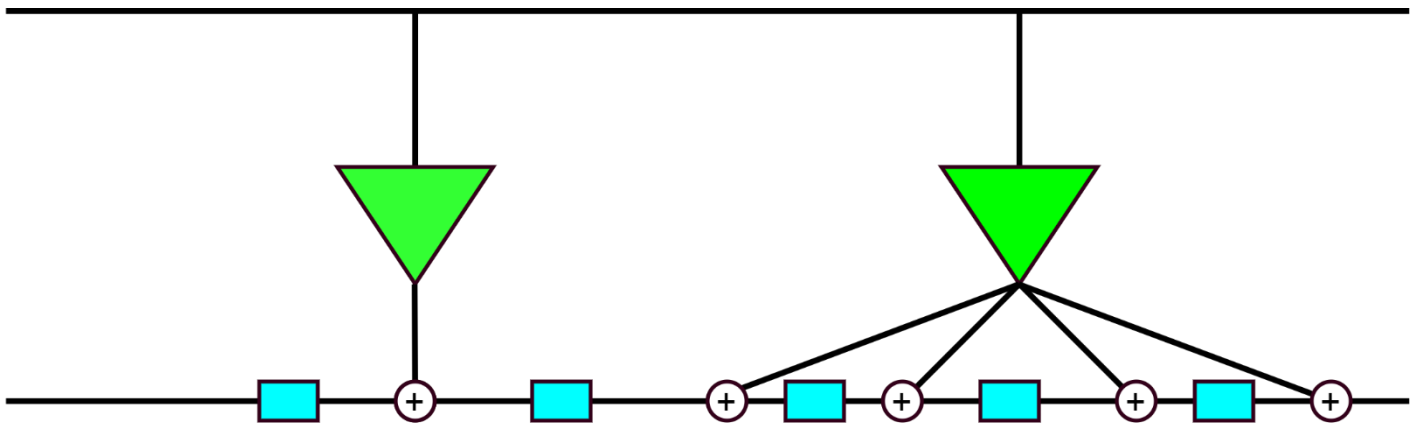
TASK – 5 :

Presentation of results for a working and optimized design layout using Cadence Innovus

New Design A

- Using only 2 multipliers
- Ripple Carry Adder



High Voltage Threshold (HVT)

Library (V)	Leakage Power (W)	Dynamic Power (W)	Slack	Metric
1.3	0.000000227	0.01414	-0.1430	
1.2	0.000000174	0.01230	-0.2335	
1.1	0.000000139	0.01146	-0.6012	
1.0	0.000000109	0.00975	-1.1413	

Low Voltage Threshold (LVT)

Library (V)	Leakage Power (W)	Dynamic Power (W)	Slack	Metric
1.3	0.0000160	0.01062	**0.0018**	**3.25×10^{8}**
1.2	0.0000133	0.00953	-0.0008	
1.1	0.0000134	0.00900	-0.0017	
1.0	0.0000101	0.00797	-0.0041	

Standard Voltage Threshold (SVT)

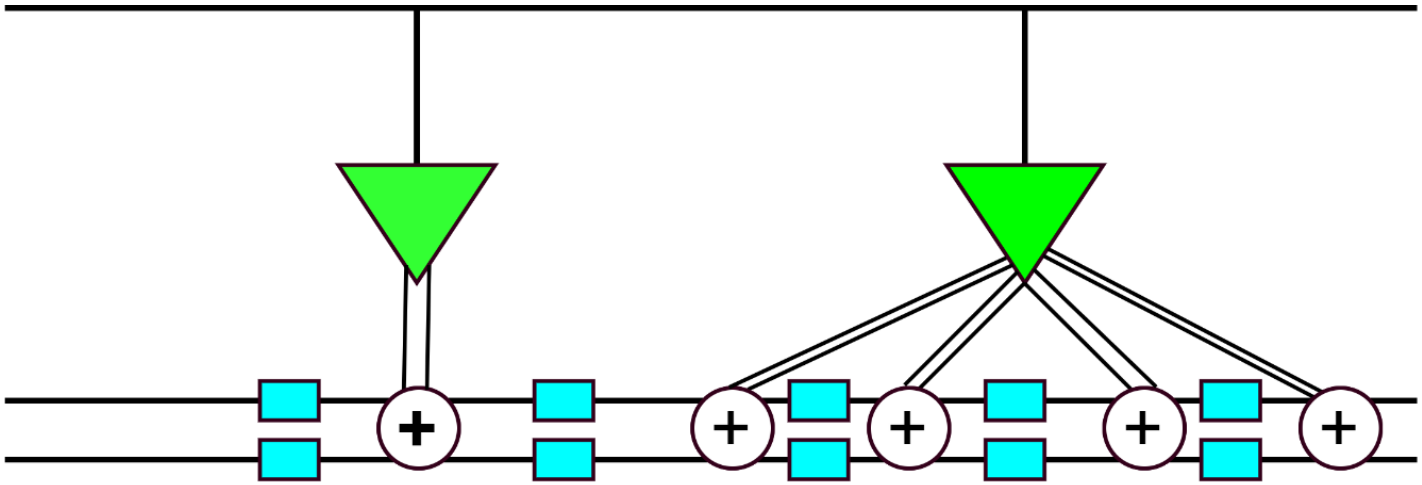
Library (V)	Leakage Power (W)	Dynamic Power (W)	Slack	Metric
1.3	0.00000166	0.01259	-0.0010	
1.2	0.00000157	0.01194	-0.0051	
1.1	0.00000130	0.01018	-0.0571	
1.0	0.00000104	0.00853	-0.2039	

All Voltage Libraries

Library (V)	Leakage Power (W)	Dynamic Power (W)	Slack	Metric
1.3	0.000013	0.01045	**0.0020**	**4.11×10^{8}**
1.2	0.000013	0.00957	**0.0009**	**4.47×10^{8}**
1.1	0.000014	0.00930	-0.0011	
1.0	0.000011	0.00836	-0.1049	

New Design B

- Using only 2 multipliers
- Carry Save Adder (4 to 2 Reduction)
- Carry-Lookahead Adder



High Voltage Threshold (HVT)

Library (V)	Leakage Power (W)	Dynamic Power (W)	Slack	Metric
1.3	0.000000233	0.0202	-0.0020	
1.2	0.000000171	0.0173	-0.0435	
1.1	0.000000125	0.0144	-0.0612	
1.0	0.000000092	0.0120	-0.0708	

Low Voltage Threshold (LVT)

Library (V)	Leakage Power (W)	Dynamic Power (W)	Slack	Metric
1.3	0.0000259	0.02008	**0.0874**	**1.07×10^{8}**
1.2	0.0000186	0.01690	**0.0052**	**1.77×10^{8}**
1.1	0.0000130	0.01400	**0.0023**	**3.06×10^{8}**
1.0	0.0000092	0.01160	**0.0450**	**5.04×10^{8}**

Standard Voltage Threshold (SVT)

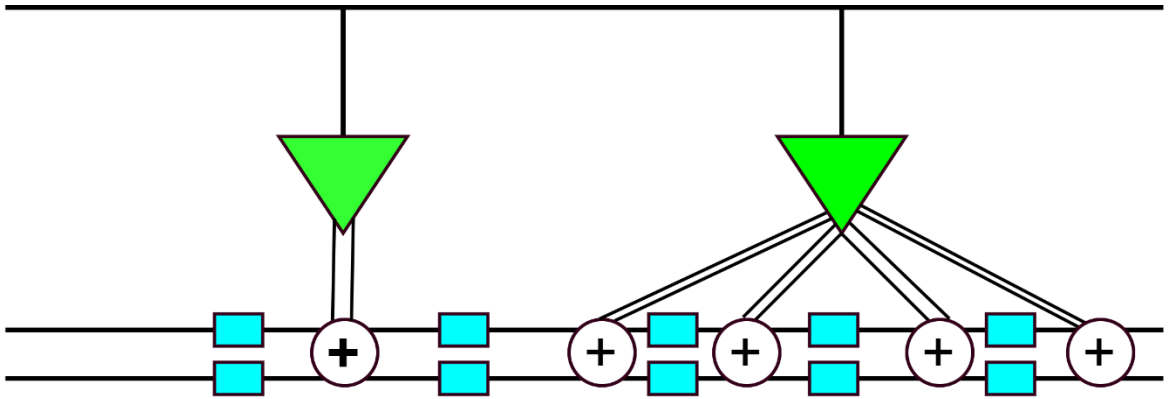
Library (V)	Leakage Power (W)	Dynamic Power (W)	Slack	Metric
1.3	0.0000019	0.0203	0.0015	1.444×10^{9}
1.2	0.0000015	0.0171	0.1332	2.171×10^{9}
1.1	0.0000011	0.0142	0.0005	3.5659×10^{9}
1.0	0.000000872	0.0117	-0.0189	

All Voltage Libraries

Library (V)	Leakage Power (W)	Dynamic Power (W)	Slack	Metric
1.3	0.000025	0.02011	0.0874	1.10×10^{8}
1.2	0.000018	0.01602	0.0007	1.93×10^{8}
1.1	0.000013	0.01409	0.0003	3.04×10^{8}
1.0	0.000009	0.01162	-0.0032	

New Design B in Synopsys

Values for ASIC	SVT 1.1 volts
Frequency	1000 MHz
Dynamic Power	14.2 mW
Leakage Power	1.14 uW
Attenuation	55.7



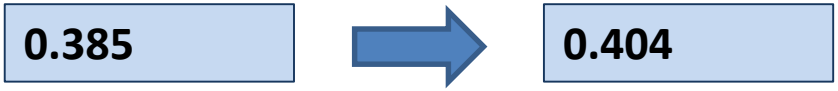
New Design B in Cadence

Parameters	Values
Dynamic Power (Watt)	0.0176487
Leakage Power (Watt)	0.0000011152
Pipeline Stages	2+1
Core Size	17598.633 μm^2
Core Utilization	0.900143
Effective Utilization	9.0024×10^{-1}
Attenuation	55.7
Metric	2.83×10^{9}

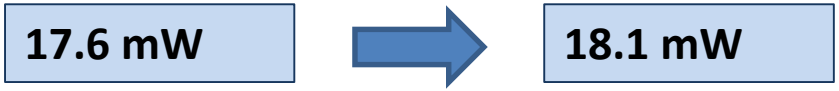
Observation

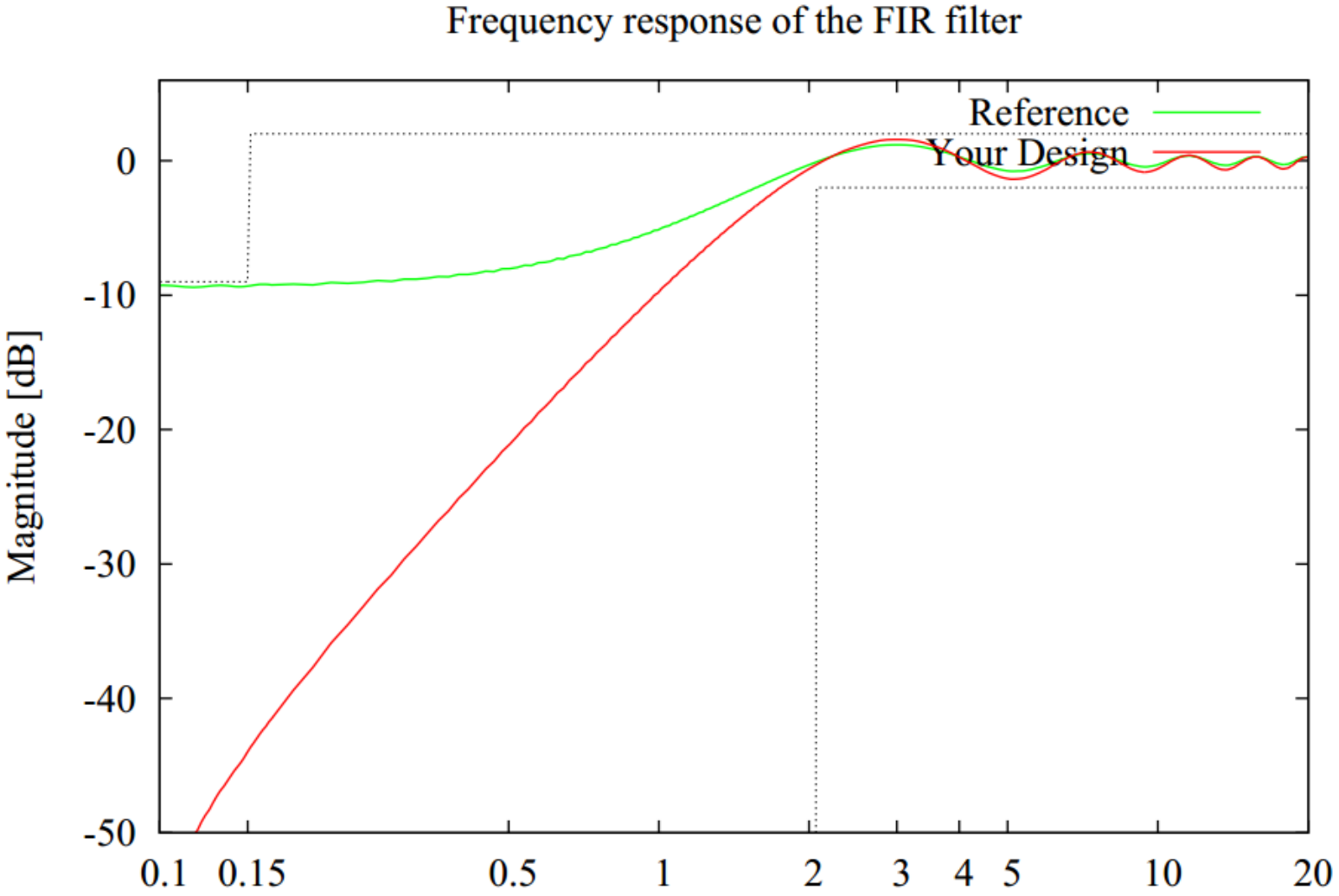
Reducing Core Ulitization from 90% to 60%

- Slack increases

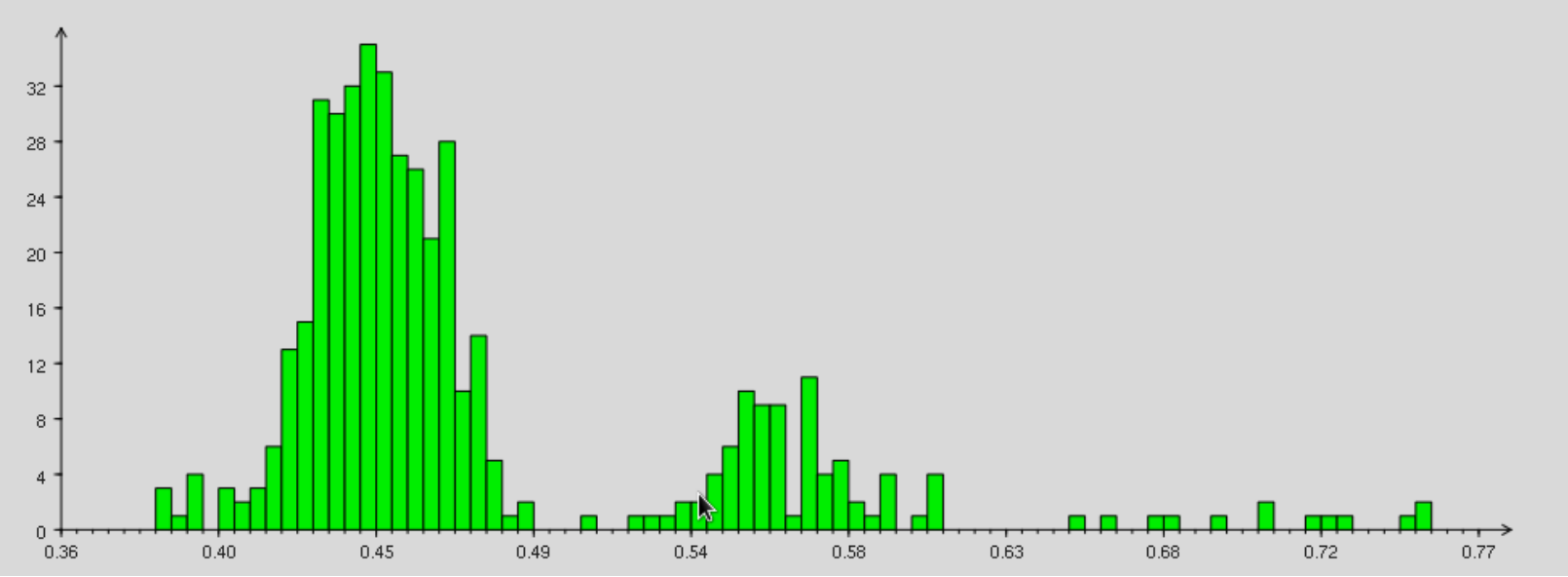


- Dynamic Power increases

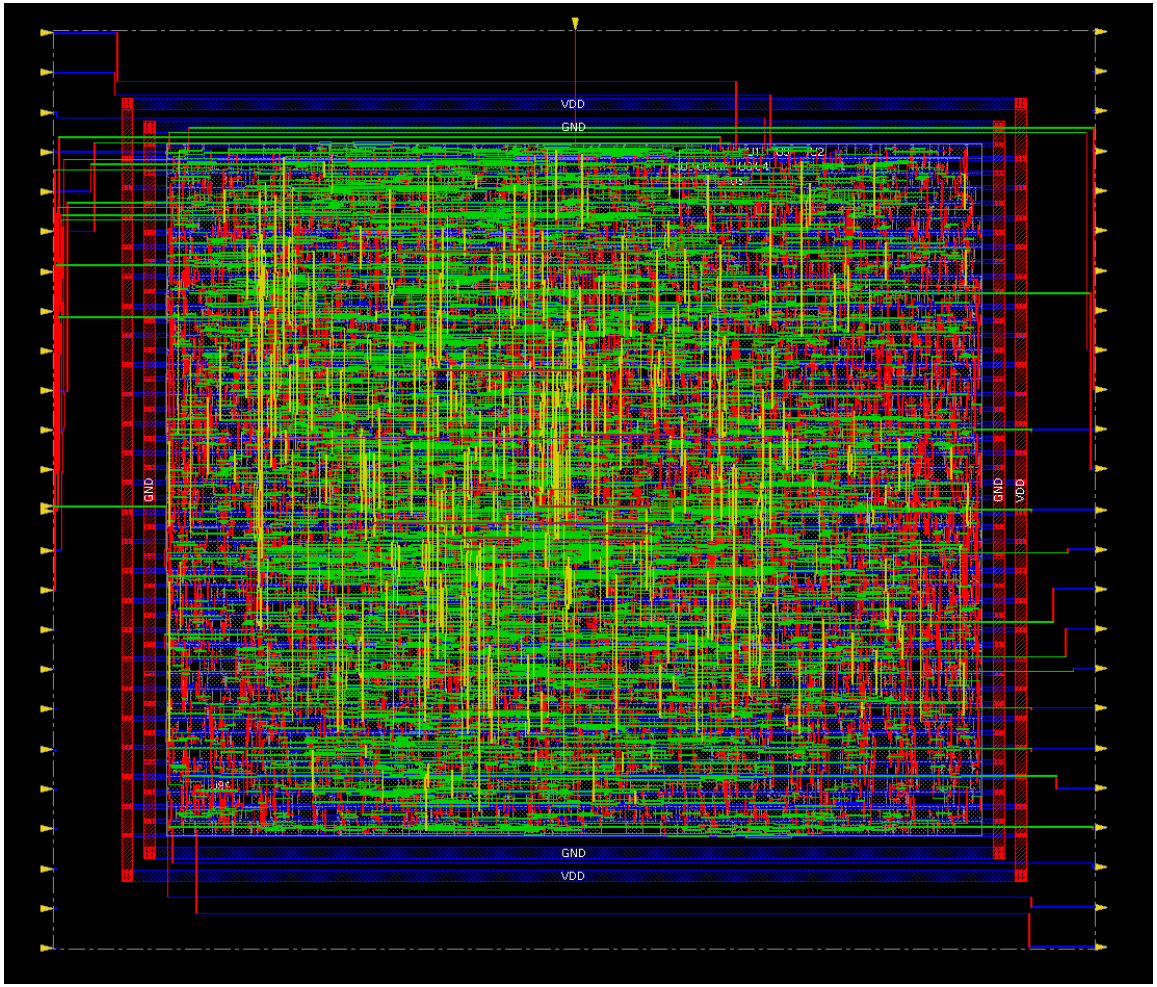



Frequency response of the FIR filter
Reference
Your Design
Magnitude [dB]
0
-10
-20
-30
-40
-50
0.1
0.15
0.5
1
2
3
4
5
10
20

Filter Slack Histogram



Final Layout



THANK YOU