Advanced VLSI Design (Module 24151)

Course and contest

Phase 5
Cadence Innvous Digital Implementation running at 1GHz

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Idea

- **To improve Direct Form I – just for fun ☺**

$$y = \sum_{k=0}^{20} h_k x[20-k]$$

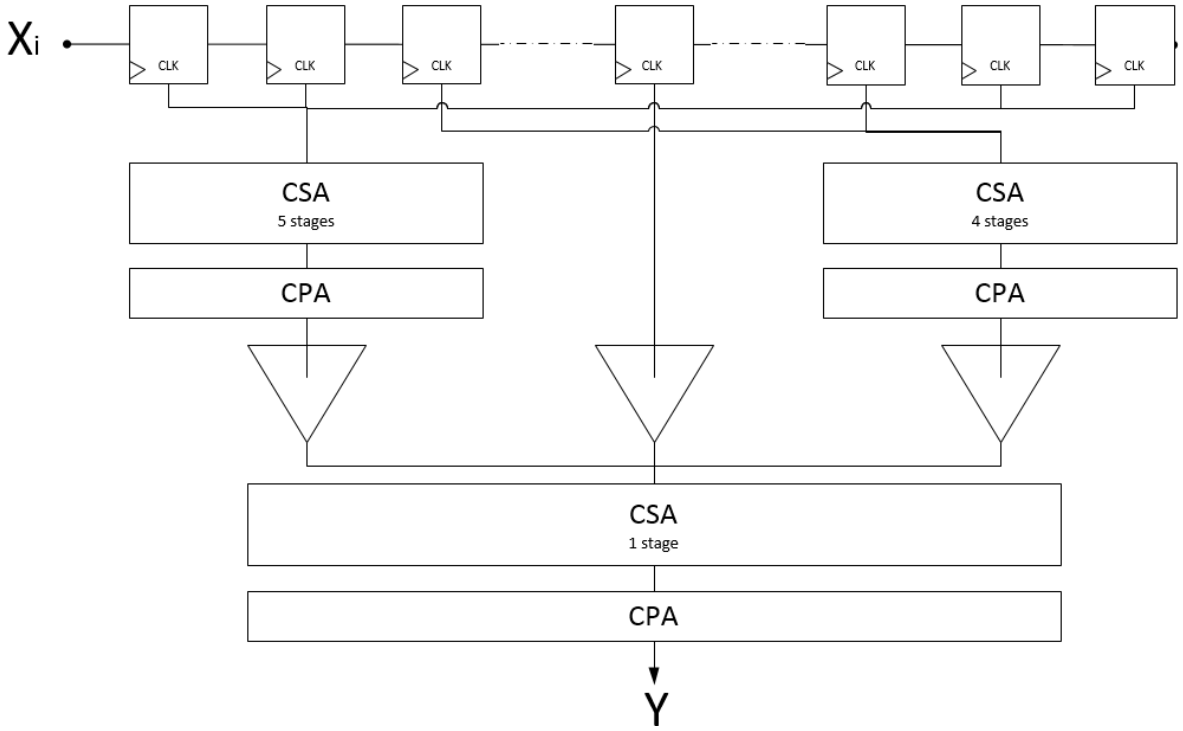
Only 3 different coefficients
(h_0, h_1, h_2)

$$y = h_0\left(\sum_{i=15}^{20} x[i] + \sum_{j=0}^{5} x[j]\right) + h_1 x[10] + h_2\left(\sum_{i=11}^{14} x[i] + \sum_{j=6}^{9} x[j]\right)$$

Idea

- **Improved Direct Form I:**

$$y = h_0\left(\sum_{i=15}^{20} x[i] + \sum_{j=0}^{5} x[j]\right) + h_1 x[10] + h_2\left(\sum_{i=11}^{14} x[i] + \sum_{j=6}^{9} x[j]\right)$$



Idea

- **Improved Direct Form I:**

		DF I	Improved DF I
FPGA	Frequency (MHz)	11.15 MHz	88.89 MHz
	Area (#LUT+#FF)	10,712	765
	Pipeline Stages	2	2

Cadence implementation

- **Comparison of different adders**
  - Direct Form II
  - Multiplier with 16 bits input / output
  - 16 bits adder

	Synopsys	Cadence	Synopsys	Cadence	Synopsys	Cadence
	1.3V HVT		1.3V HVT		1.3V HVT	
Dynamic power (mW)	10.4501	15.6459	10.8613	16.3908	10.352	15.5096
Leakage power (nW)	146.1925	150.2099	151.0663	154.6512	143.1166	146.4008
Adder	**CLA**		**CSeA**		**RCA**	

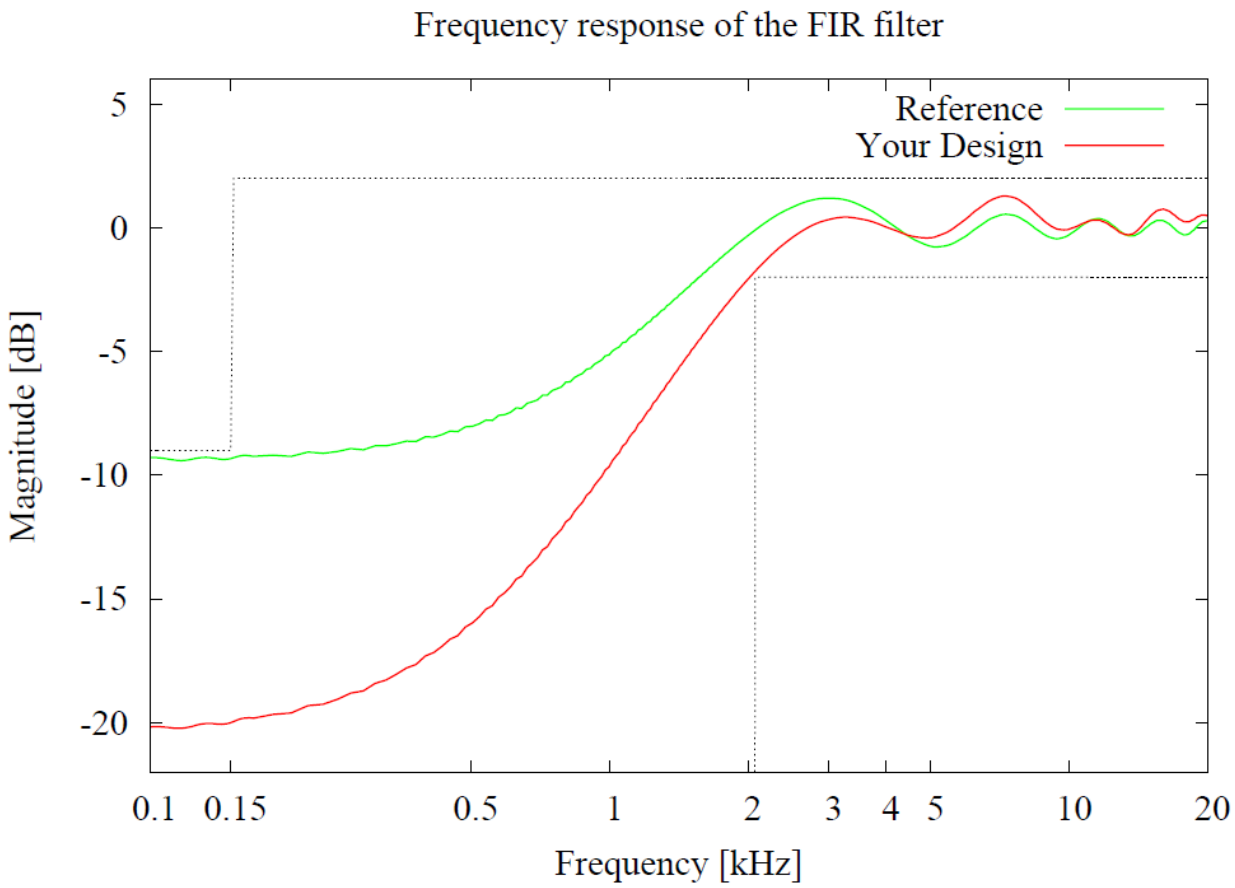
Cadence implementation

- **Final design**
  - Direct Form II
  - 16 bits multiplier
  - 16 bits RCA adder
- **Synthesis**
  - 1.3V HVT
  - compile_ultra with high timing effort
- **Cadence parameters**
  - Ratio (H/W): 1.16
  - Core utilization: 59.9 %
  - Core size: 24’021.28 um^2

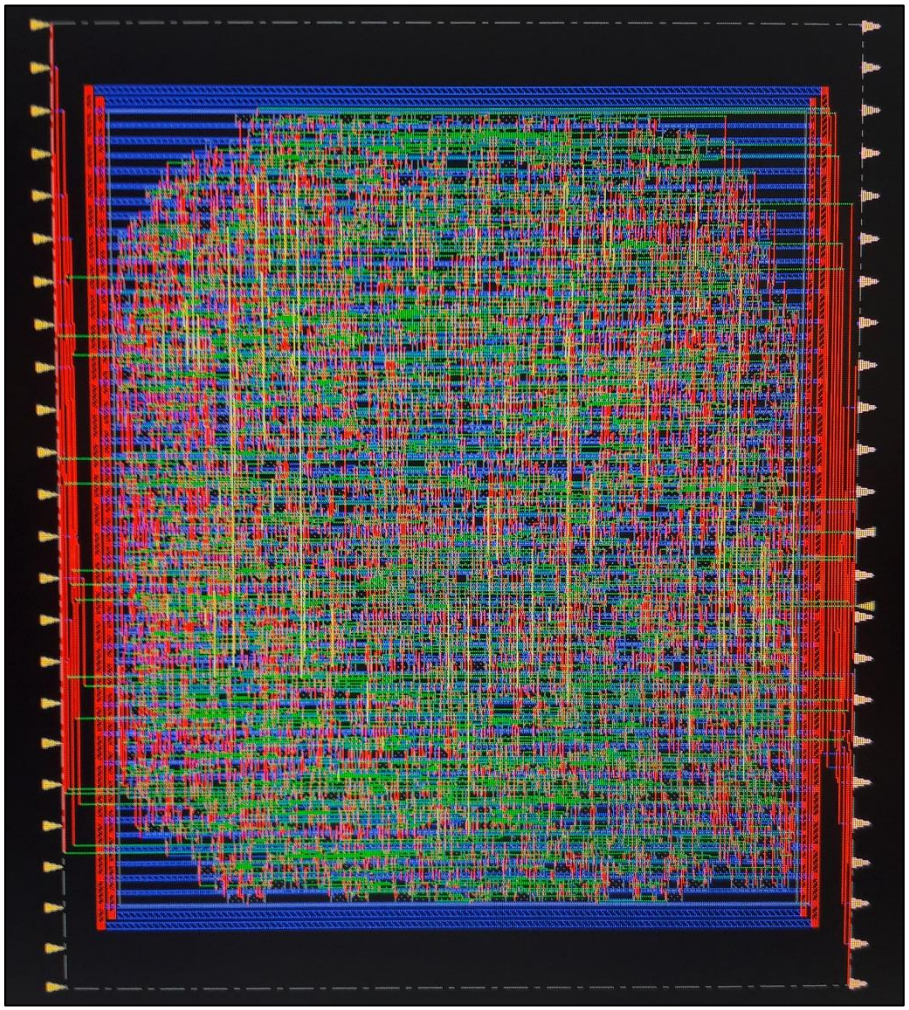
Metric for ASIC	
Frequency (MHz)	1'001 MHz
Dynamic Power	15.51 mW
Leakege Power	146.40 nW
Pipeline Stages	3
Attenuation (dB)	19.84 dB
Metric	8.739E+09

Frequency response

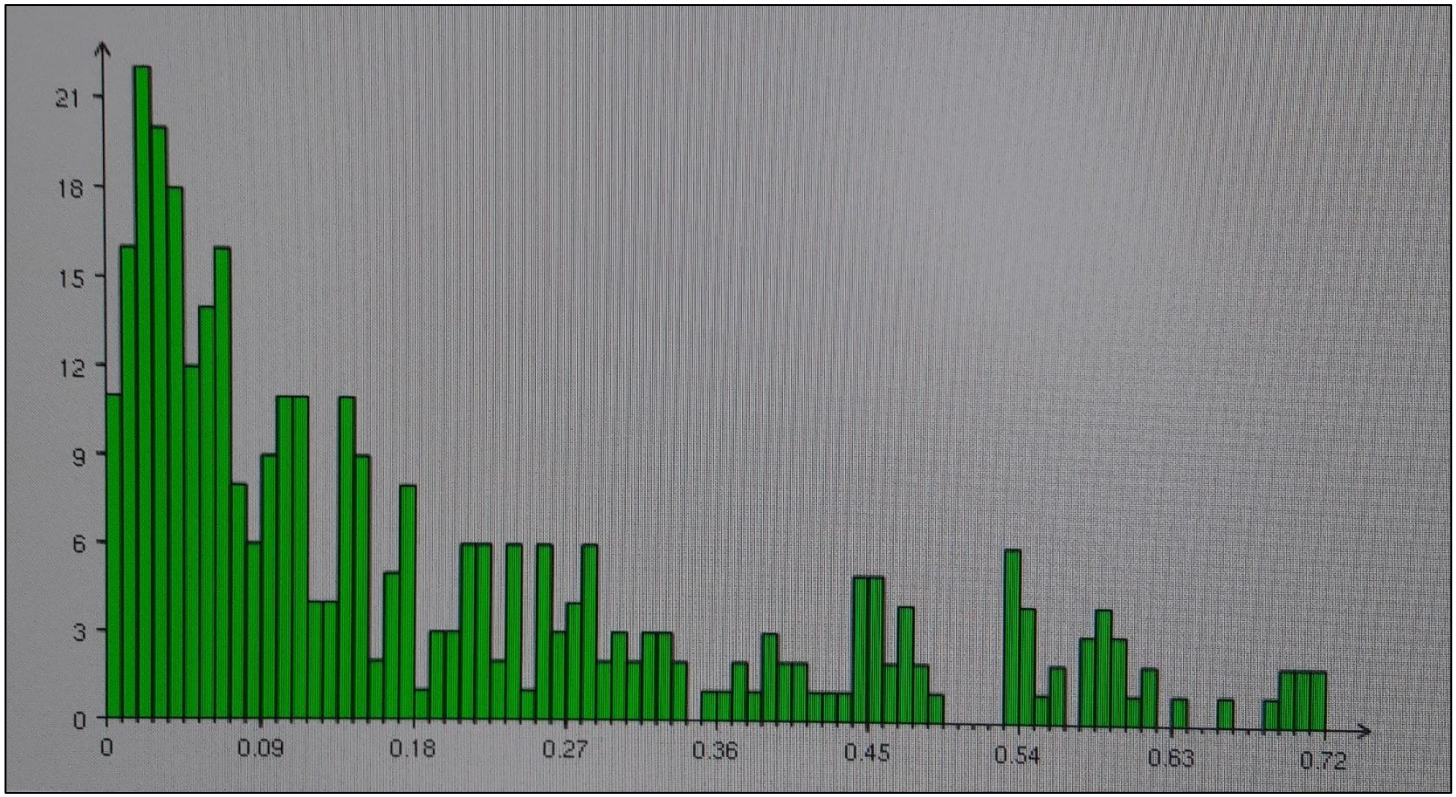
Achieved attenuation: -19.843 dB



Chip layout



Path histogram



Overview

		Phase 1	Phase 2	Phase 3	Phase 4	Phase 5
FPGA	Frequency (MHz)	11.15 MHz	166.67 MHz	128.21 MHz	153.85 MHz	153.85 MHz
	Area (#LUT+#FF)	10,712	5,109	972	654	644
	Pipeline Stages	2	4	3	3	3
	Attenuation (dB)	9.315 dB	9.177 dB	19.842 dB	19.838 dB	19.838 dB
	Metric	7.578E-12	6.882E-11	2.161E-08	7.092E-08	7.427E-08
ASIC	Frequency (MHz)				1'000 MHz	1'001 MHz
	Dynamic Power				15.57 mW	15.51 mW
	Leakege Power				1.44 uW	146.40 nW
	Pipeline Stages				3	3
	Attenuation (dB)				19.84 dB	19.84 dB
	Metric				8.850E+08	8.739E+09

Overview

Implementation of Direct Form I at phase 1

~ 8 days

Implementation of improved Direct Form I

~ half day (5 hours)

Thank you for your attention.
Q & A?