Universität Rostock Traditio et Innovatio

Institut für Angewandte Mikroelektronik und Datentechnik

Selected Topics in VLSI Design (Module 24513)

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Presentation on Task 5

Presentation of results for a working and optimized design layout

Previous Design

- 24 bit Carry Select Adder.
- 2 Multipliers (Similar Coefficients / Multiplier Reduction).

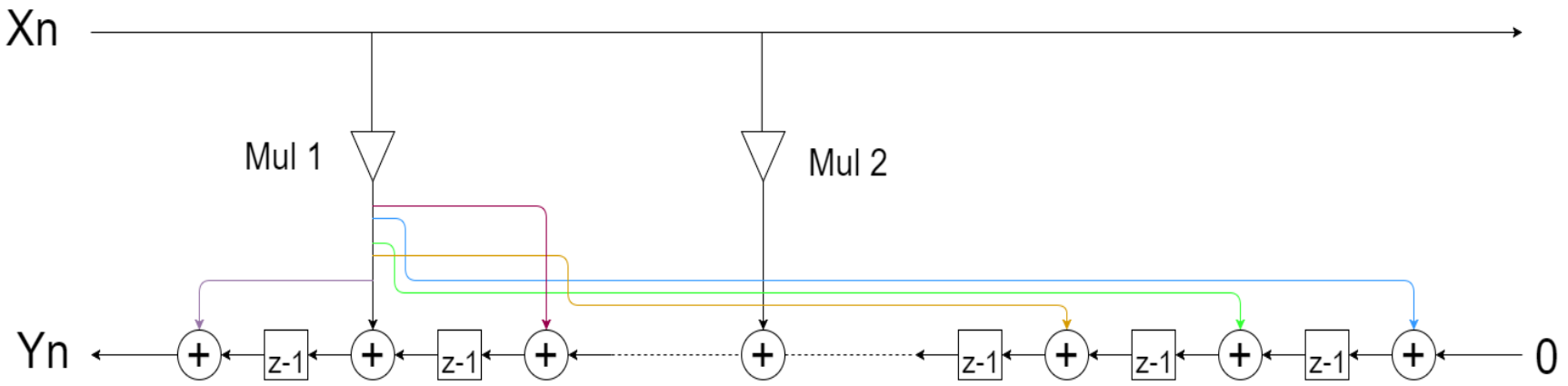
Target

- Optimized Design.
- Better Metric.
- Final Chip Layout.

2 Multipliers

- Taking 17 Most Significant Bits.
- Increased Coefficients of MUL 1 for better attenuation.

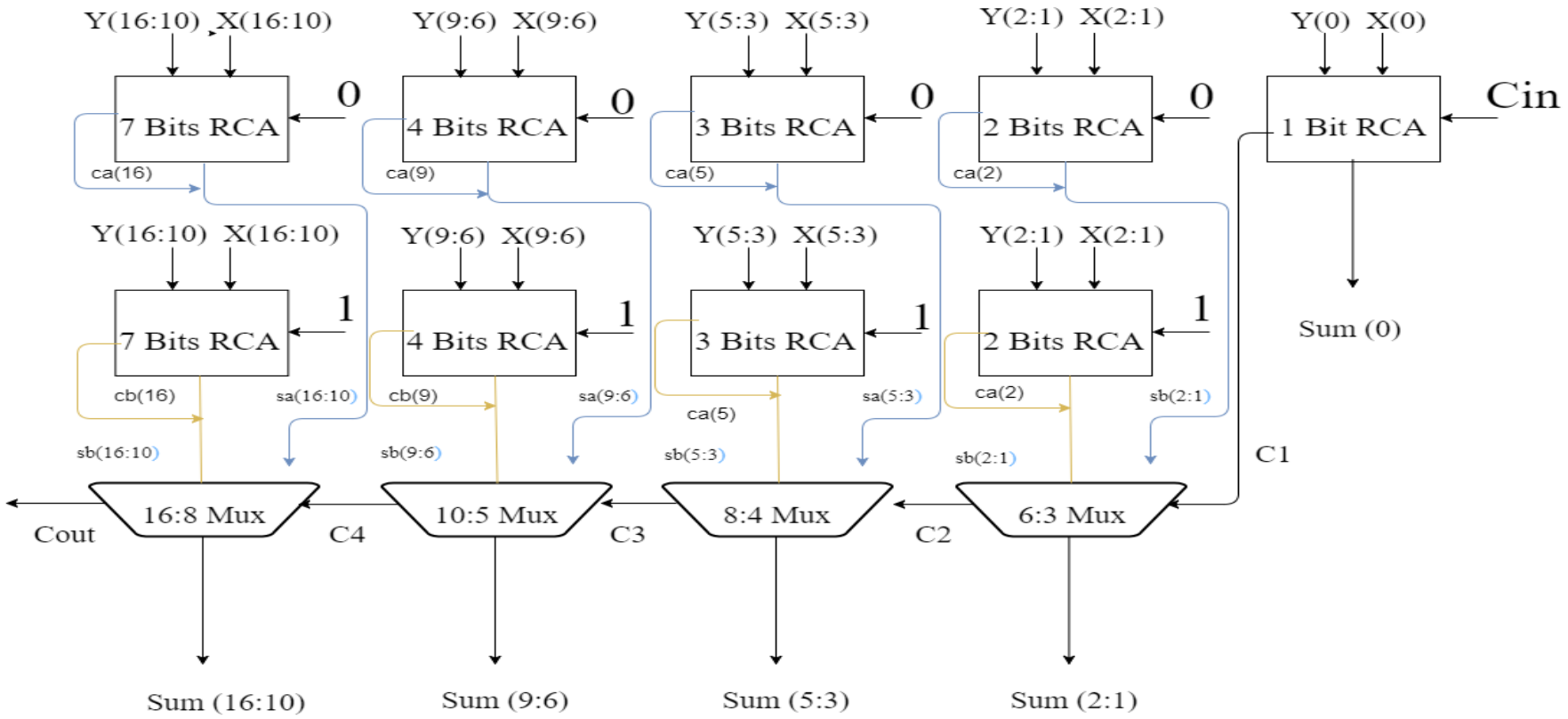
Coefficient 0,20 (same)	Coefficient 1,19 (same)	Coefficient 2,18 (same)	Coefficient 3,17 (same)	Coefficient 4,5,15,16 (same)	Coefficient 6,7,13,14 (same)	Coefficient 8,9,11,12 (same)	Coefficient 10
MUL 1	**MUL 1**	**MUL 1**	**MUL 1**	**MUL 1**	**MUL 1**	**MUL 1**	**MUL 2**



2 Multipliers for Coefficients

17 Bit Carry Select Adder

- FIR filter data out is of 24 bits.



17 Bit Carry Select Adder

Improved Results On Synopsys

Target Achieved

- Optimized Design (P_{dyn} & P_{leak})
- Better Metric.

Voltage(V) (All lib)	Slack	Dynamic Power (mW)	Cell Leakage Power (uW)	Total Area	Attenuation	Metric
1.1	0.0002	23.41	17.19	22063	-9.113888	2.2647819^7

Voltage(V) (SVT)	Slack	Dynamic Power (mW)	Cell Leakage Power (uW)	Total Area	Attenuation	Metric
1.2	0.0001	16.84	1.15	15026	-28.624541	1.4780822^9

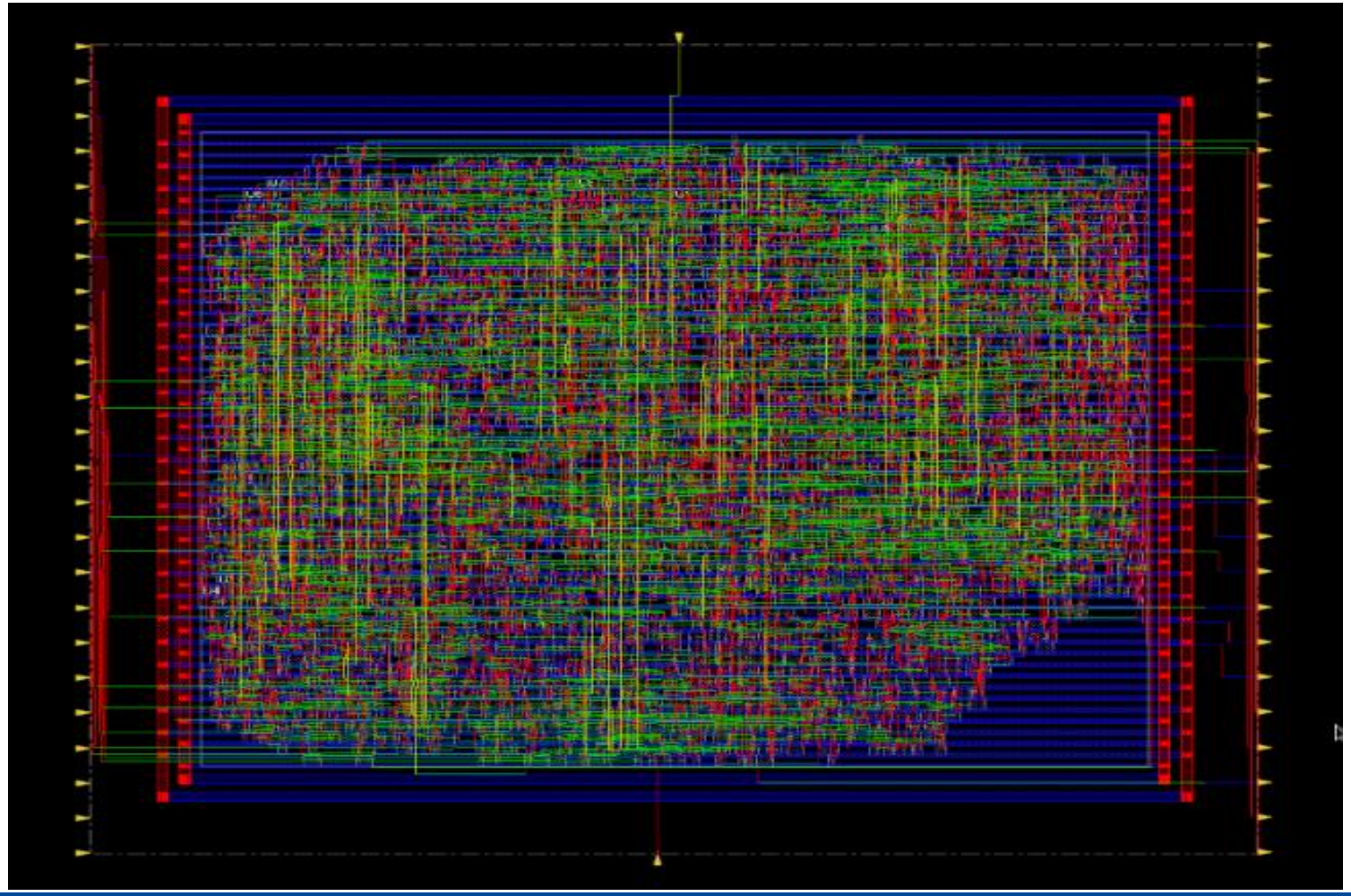
Execution Results

Implementation of Design on Cadence

- Determination of Core Utilization for Floorplanning.

Core Utilization	60%	45 %
Core Size	25045.384 um^2	33393.55 um^2 ↑
Slack	0.192	0.139 ↓
Dynamic Power	17.65 mW	18.12 mW ↑

Final Chip Layout



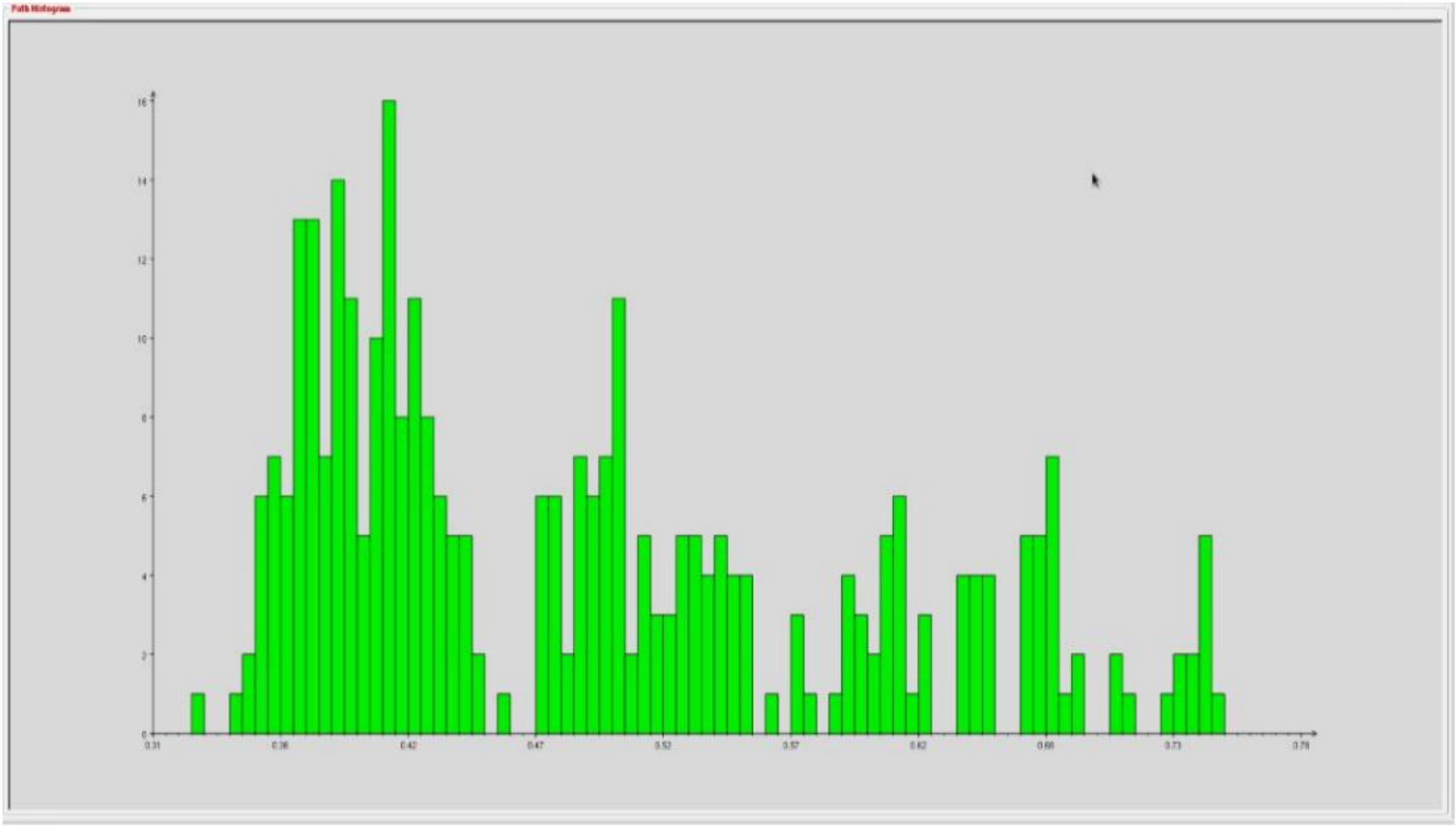
Slack Optimization

- Used ECO to increase slack (Setup time).
- Reduces Verification time.

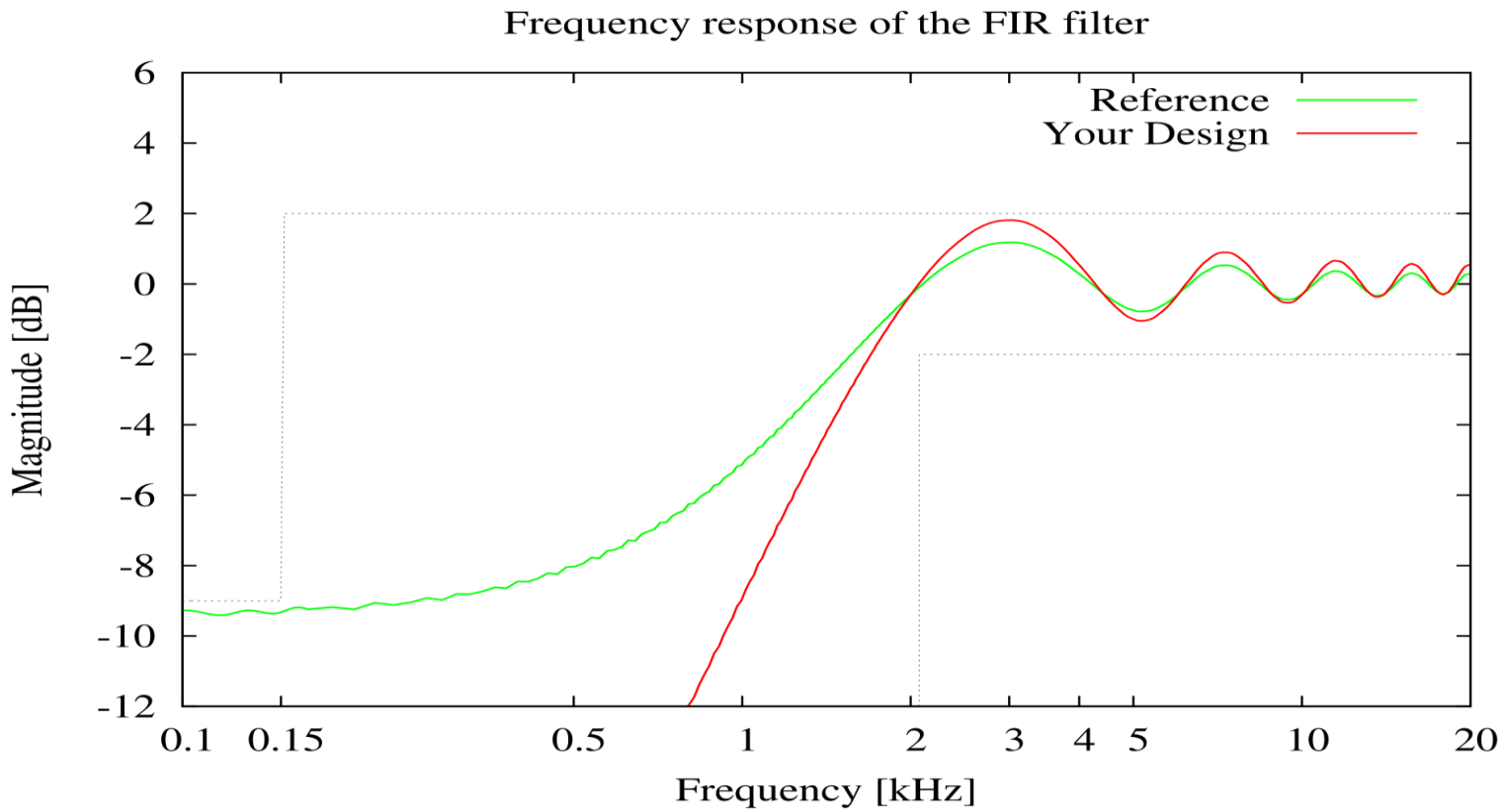
Hold Time	Setup Time
0.034	0.192

Hold Time	Setup Time
0.034	0.329

Path Histogram (Setup Time)



Frequency Response of the FIR Filter



Design Parameters

Frequency (T / F)	1 ns / 1 GHz
Power (P_{dyn} / P_{leak})	17.65 mW / 1.15 uW
Pipeline Stages	4
Attenuation	-28.624541
Metric	1.410249587 x 10^9 W^-2
Core Size	25045.384 um^2
Core Utilization	60.042 %
Total Area of Chip	39349.9 um^2

Thank You