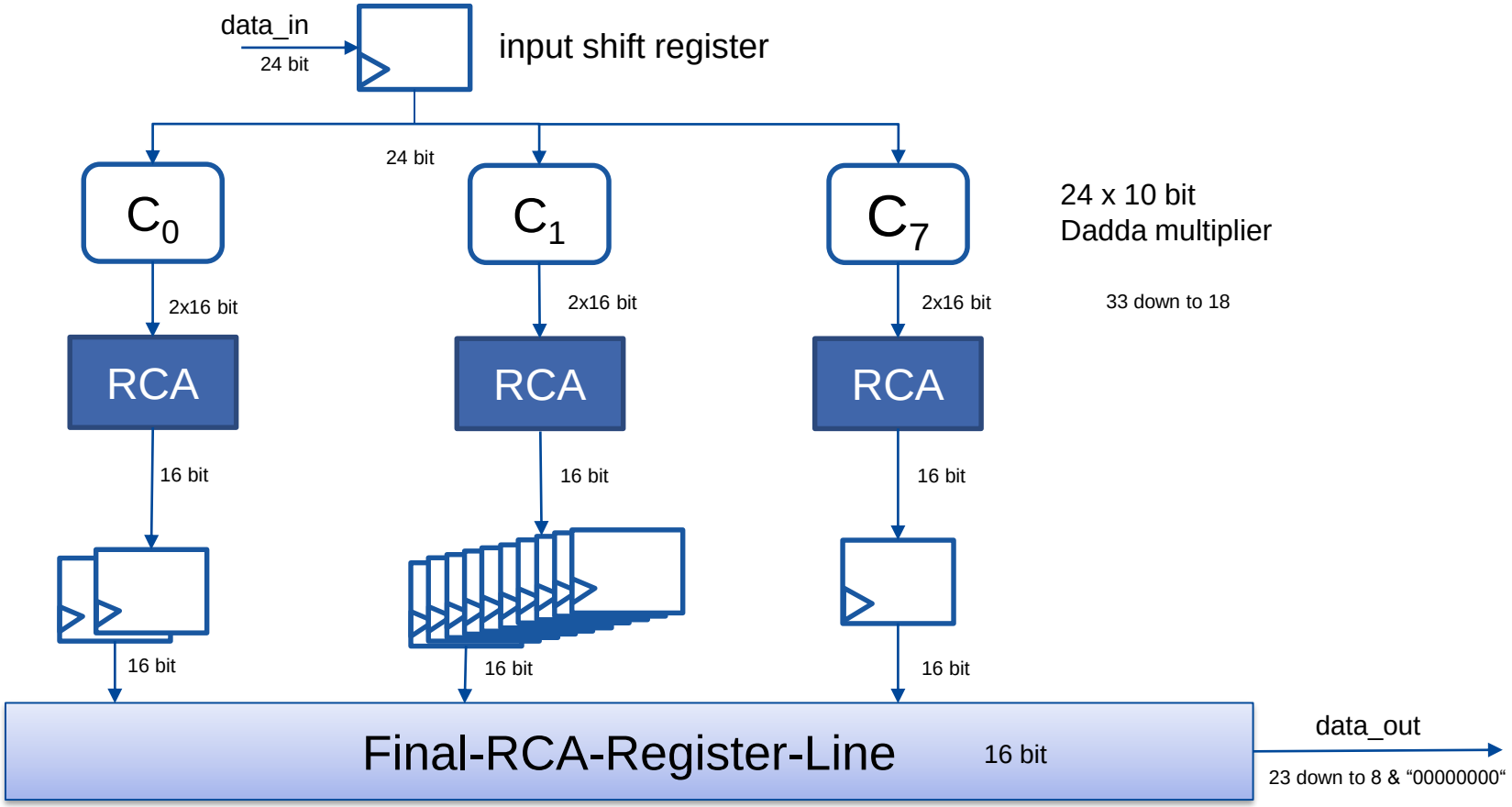
Advanced VLSI Design (Module 24151)

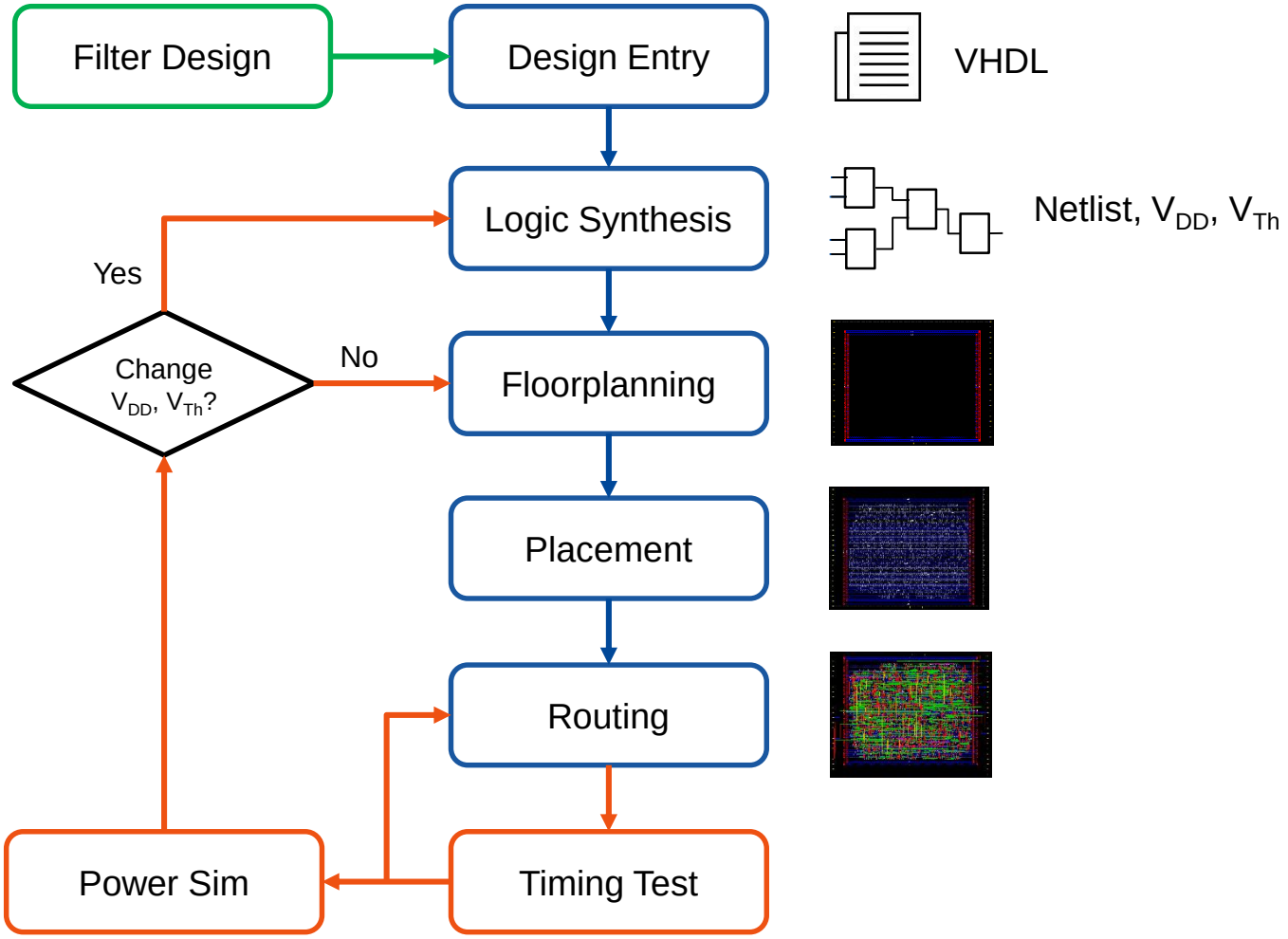
Chip Layout Phase 5

Alexander Schumann

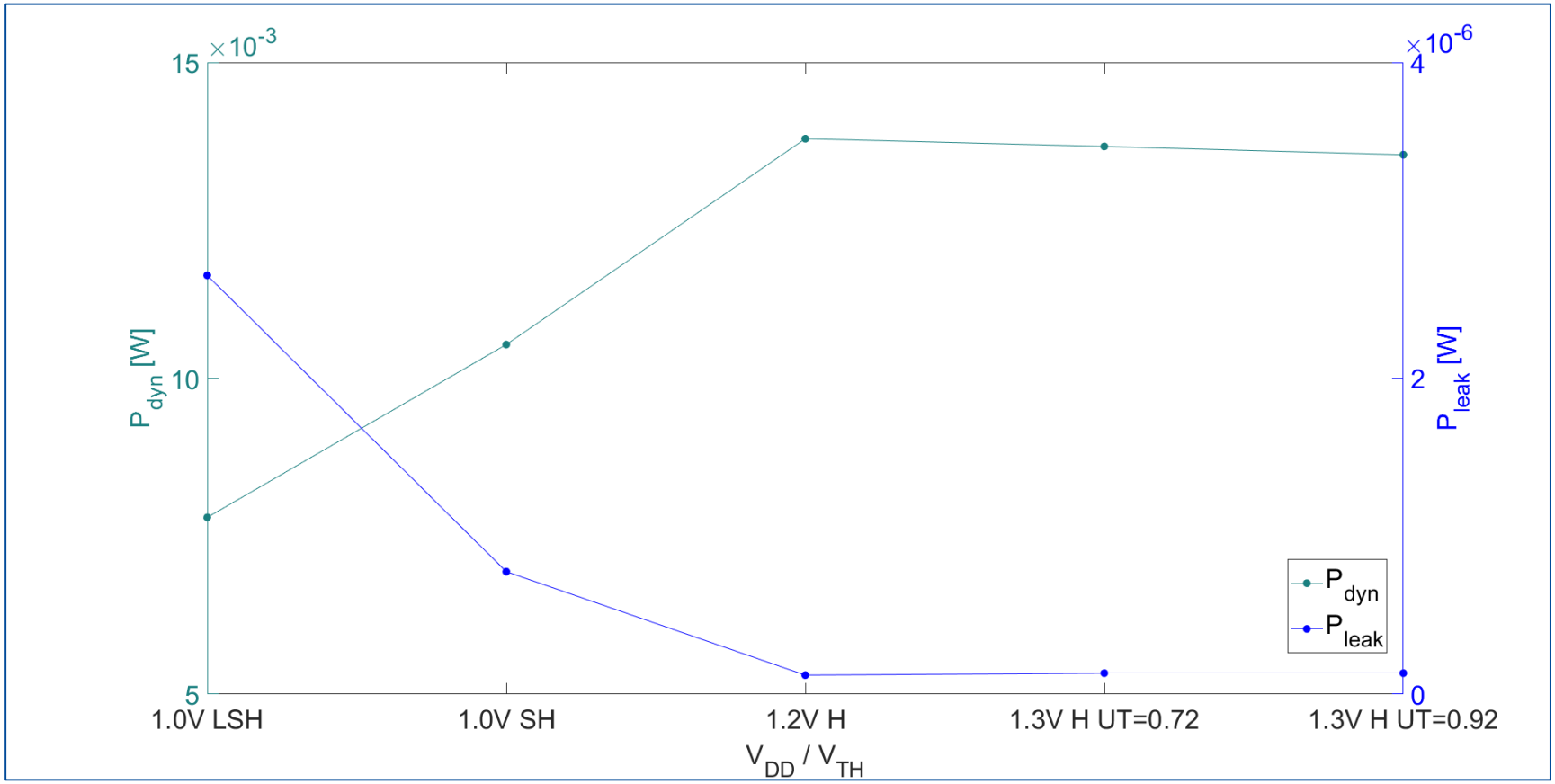
Code - Structure



Design Flow


Filter Design
Design Entry
VHDL
Logic Synthesis
Netlist, V_{DD}, V_{Th}
Yes
Change V_{DD}, V_{Th}?
No
Floorplanning
Placement
Routing
Power Sim
Timing Test

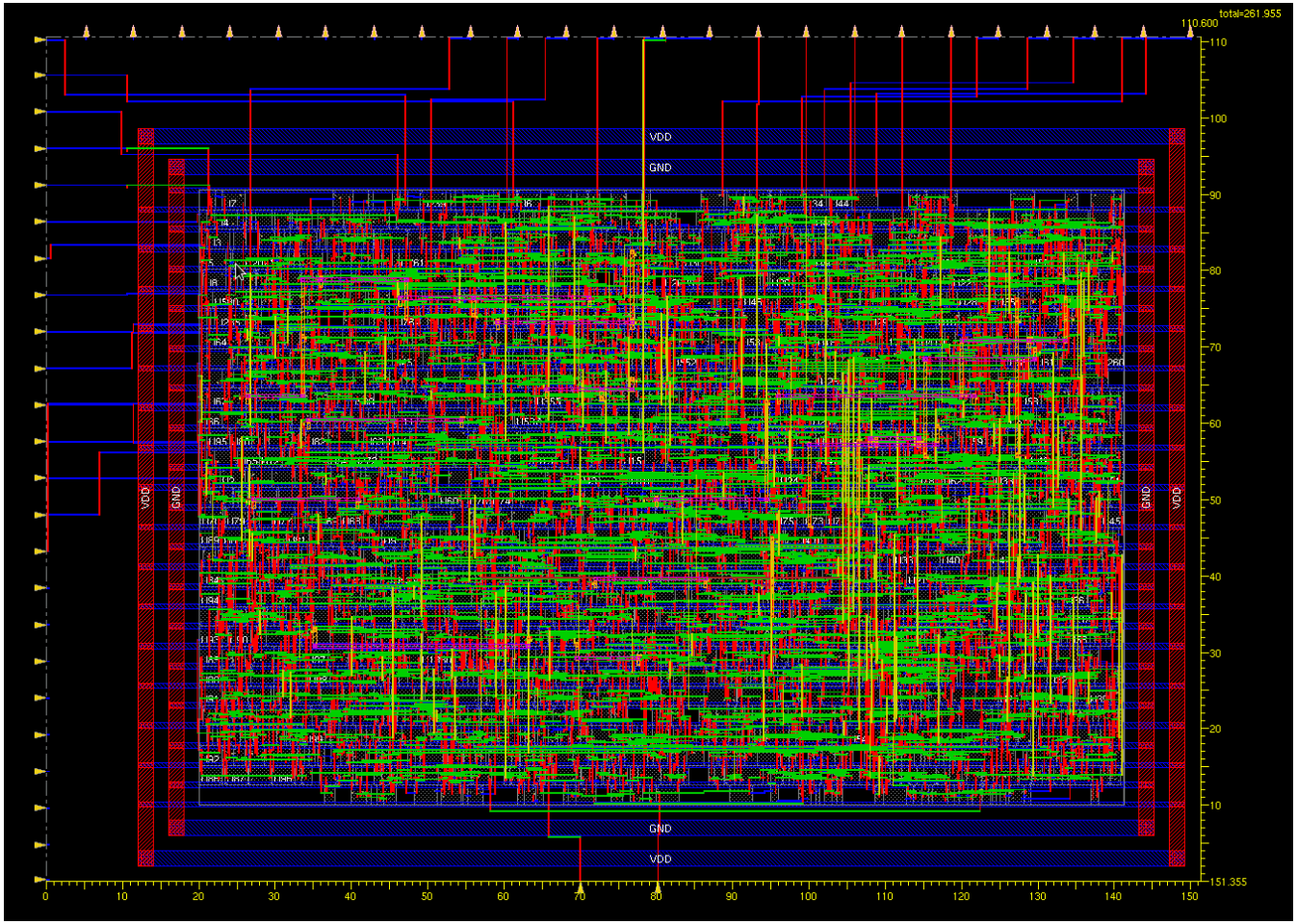
Comparison V_{DD} / V_{TH}



Comparison Power from Netlist & after Routing

	Netlist (Simulation)	After Routing
Dyn. Power 1.0 V LSH	7.43 mW	7.798 mW
Leak. Power 1.0 V LSH	2.70 µW	2.6519 µW
Dyn. Power 1.3 V H	13.2019 mW	13.5385 mW
Leak. Power 1.3 V H	133.2516 nW	133.2516 nW

1.3 V High - V_{TH}

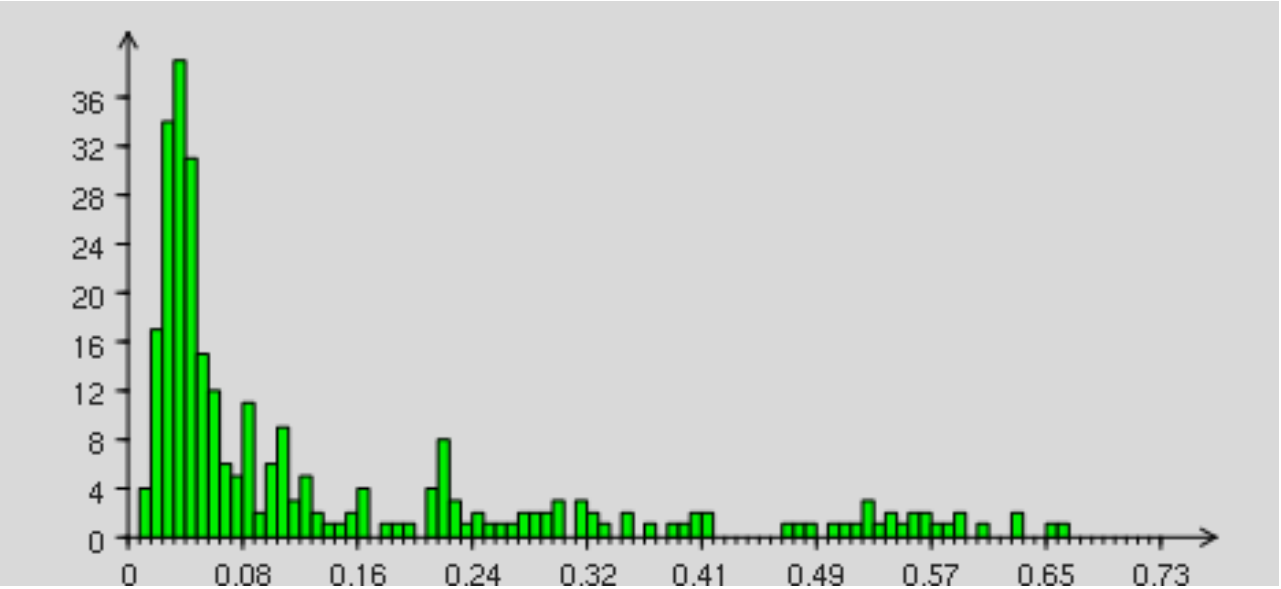

total=261.955
110.600
151.355
VDD
GND
GND
VDD
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150

Result

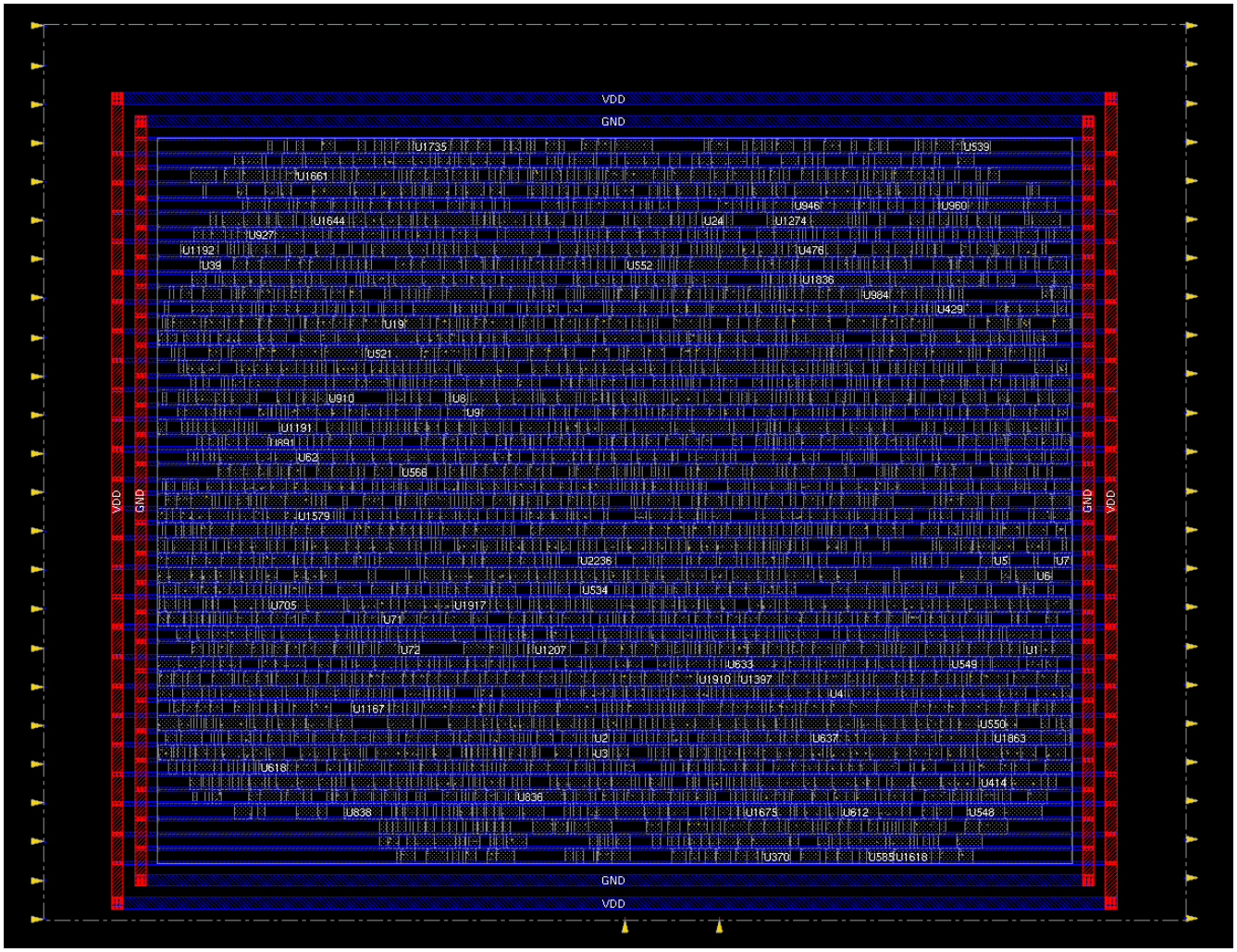
- $V_{DD} = 1.2V, \mathrm{LPHVT}$

	Values
Total Area of Chip	31605 µm²
Effective Utilization	74.123 %
Total Dynamic Power	13.7920 mW
Cell Leakage Power	120.6874 nW
Frequency	1 GHz
Attenuation	11.298800 dB
Metric	$6.78802 \cdot 10^9$

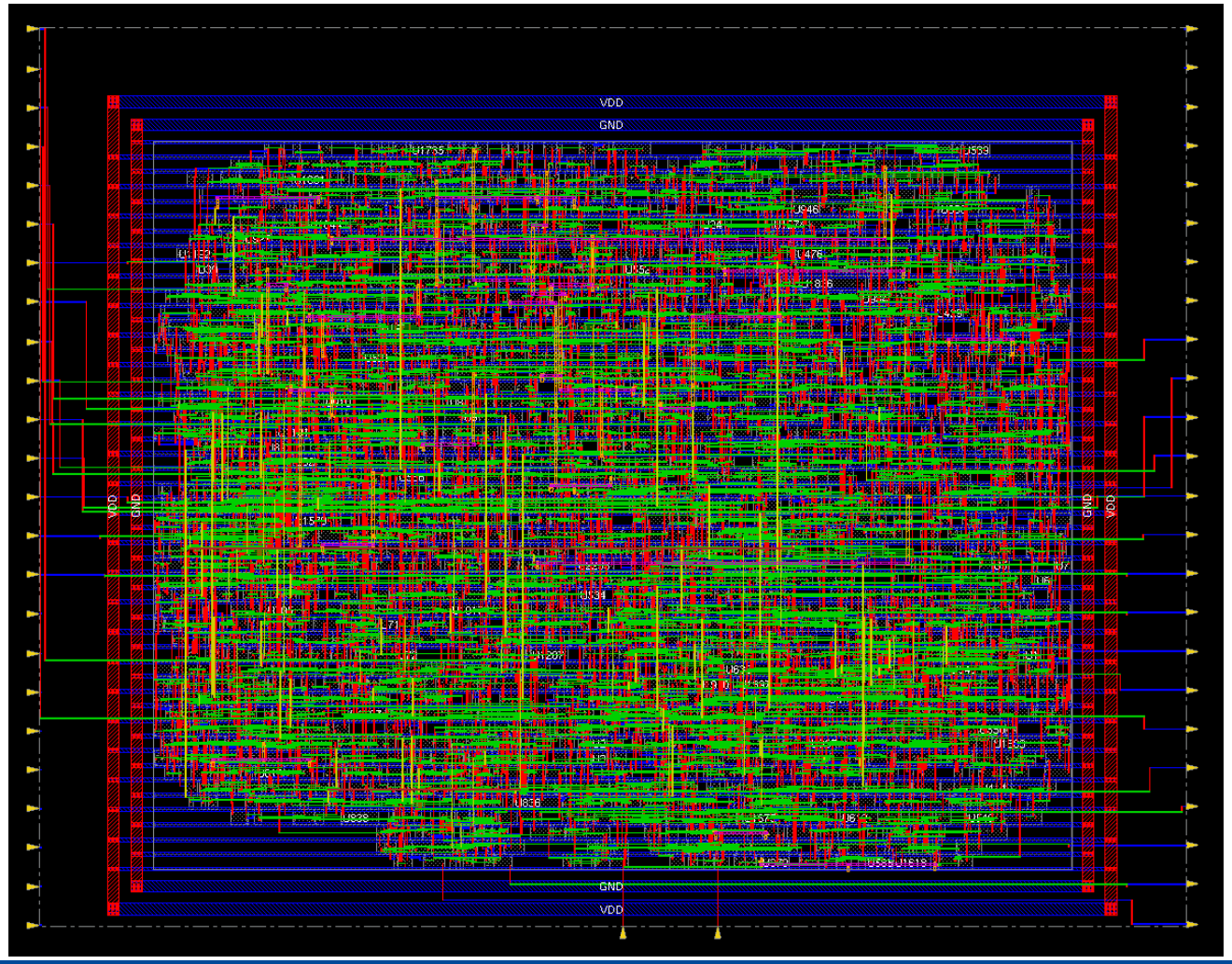
Timing Histogram



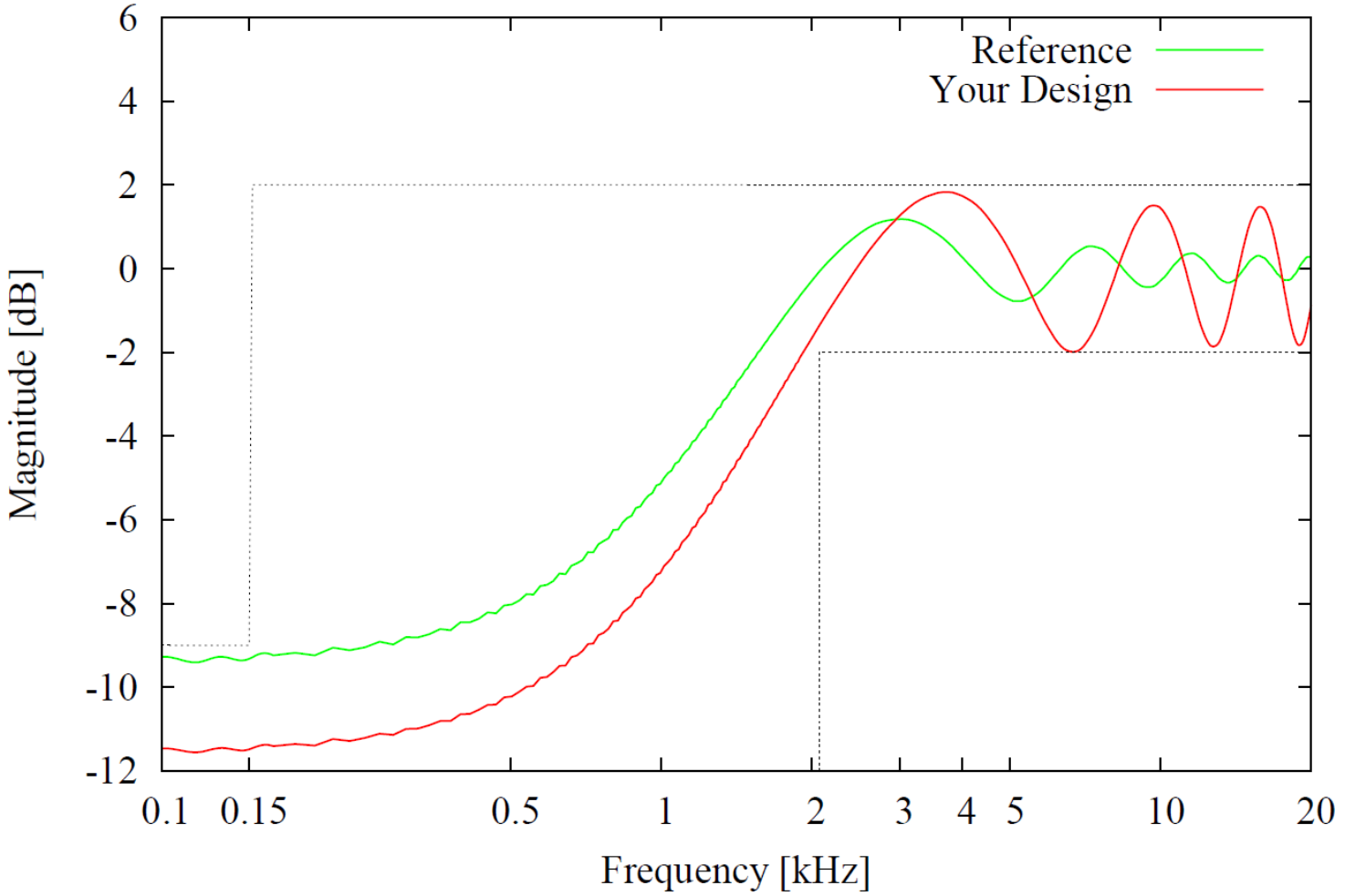
Cell Placemant



Chip Layout



Frequency Response



Thank you for your attention!