Universität Rostock Traditio et Innovatio

Institut für Angewandte Mikroelektronik und Datentechnik

Advanced VLSI (Project)

Module (24513)

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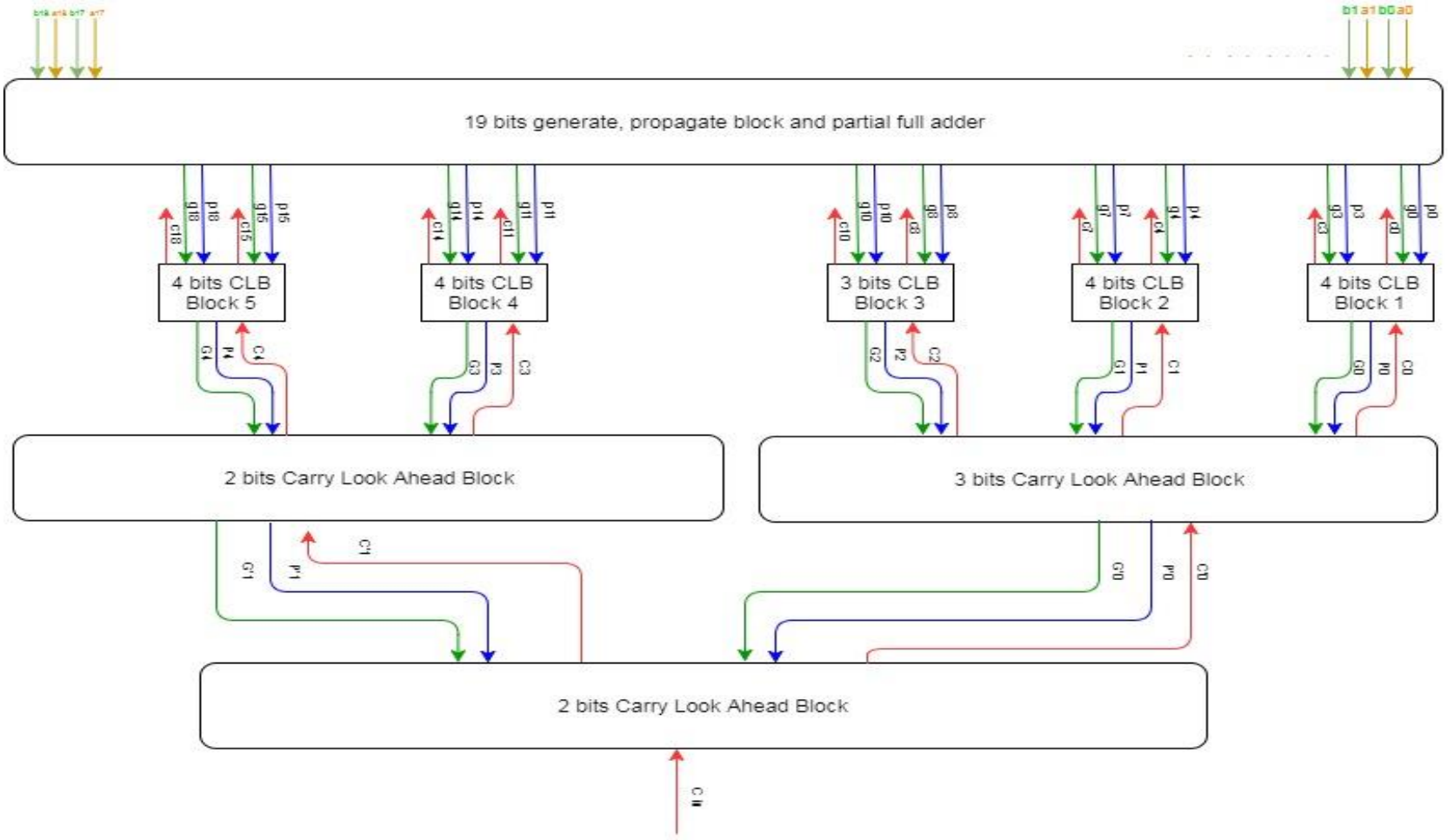
TASK – 5 :

Presentation of results for a working and optimized design layout, **running at one GHz**.

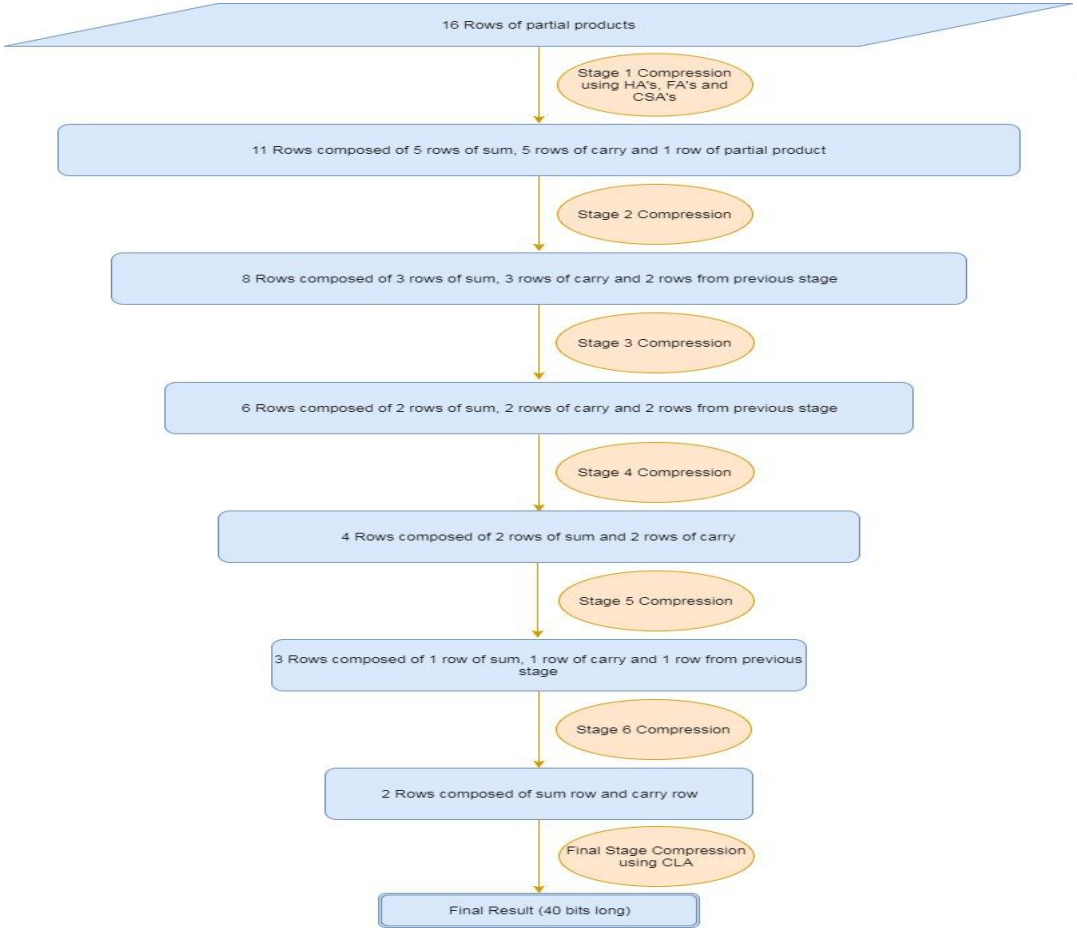
Design Improvement

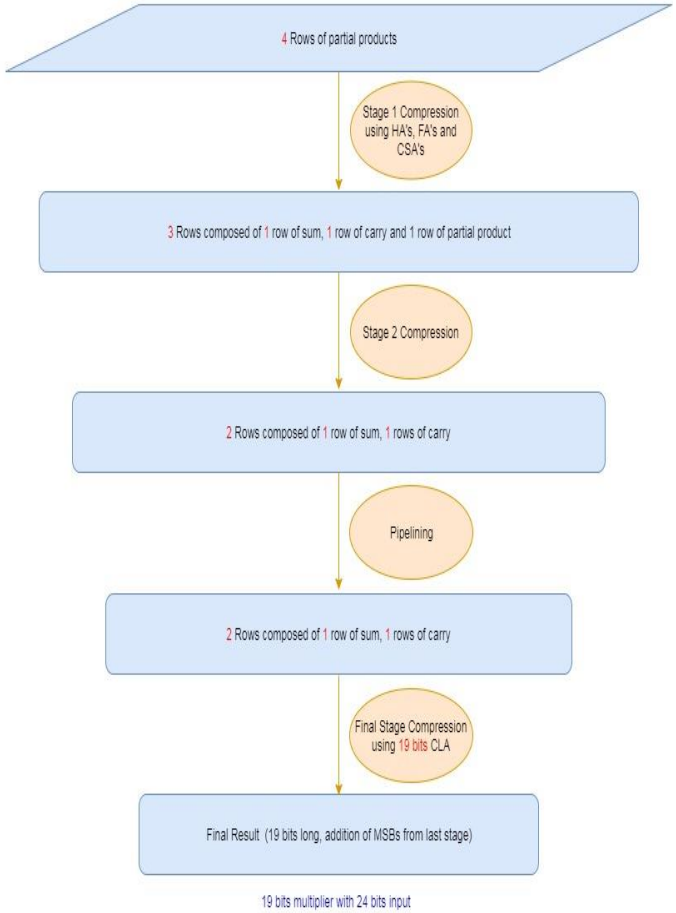
- Replacing 24 bits adder by 19 bits adder
- Changing multiplier coefficients for higher attenuation
- Use of 2 CSD multipliers (positive coefficient for multiplier 10 and same negative coefficient for all other multiplier)
- Tried to improve last design using in-built parameters, e.g., compile_ultra

19 bits CLA


19 bits generate, propagate block and partial full adder
4 bits CLB Block 5
4 bits CLB Block 4
3 bits CLB Block 3
4 bits CLB Block 2
4 bits CLB Block 1
2 bits Carry Look Ahead Block
3 bits Carry Look Ahead Block
2 bits Carry Look Ahead Block

Improvement in multiplier design





Comparison from previous result (FPGA & ASIC synthesis tool)

- Design is operable at 1.3 V and 1.2 V
- Use of single library CORESVTtyp13v at 1.3 V
- Use of different library at 1.2 V

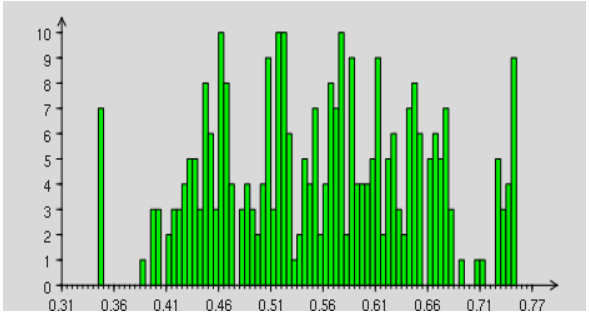
WNS	LUT	FF
2.034	936	628
3.137	649	439

Voltage	Frequency	Attenuation	Slack	Total Cell Area	Dynamic Power	Cell Leakage Power	Metric
1.3 V	1000	-9.23618	0.0014	16229.719819	24.8703 mW	1.7398 uW	2.934578042E8W^-2
1.3 V	1000	-13.959593	0.0003	12323.999846	18.1615 mW	1.3420 uW	5.727545204E8 W^-2

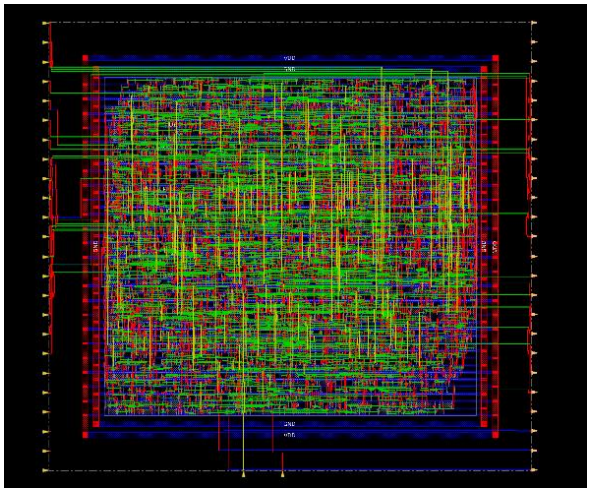
Cadence Design Parameters and Results

- Use of single library CORESVTtyp13v at 1.3 V

Achieved Attenuation	-13.959593
Timing (T_{min} / f_{max})	1 ns / 1000 MHz
Power (P_{dyn} / P_{leak})	18.6256 mW / 1.342 uW
Pipeline Stages	3
Metric	5.584830138 x 10^8 W^-2
Core Size	16432um^2
Chip Size	28299um^2
Core Utilization	74.99 %

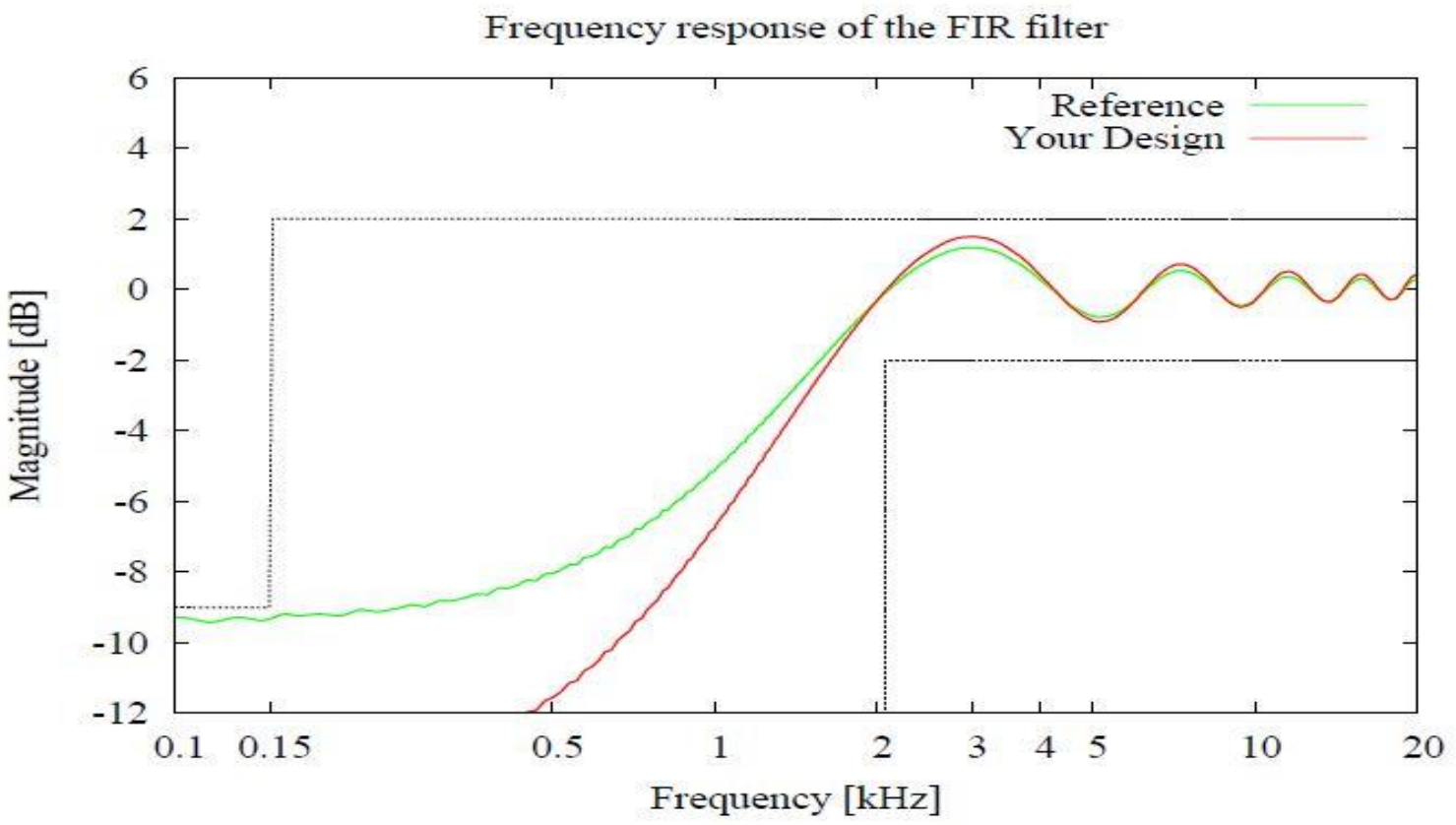


Path Histogram



Chip layout

Frequency Response



THANK YOU