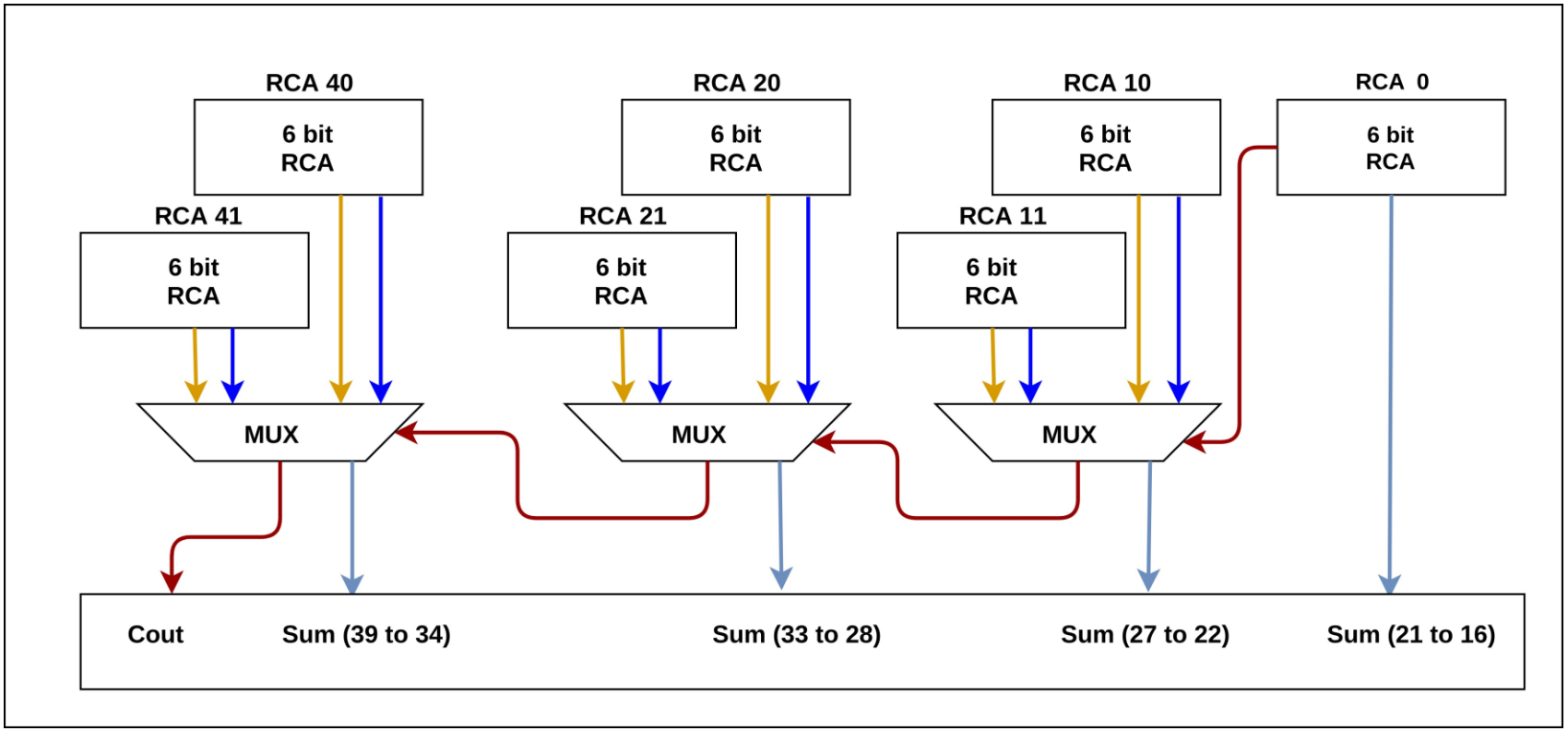
Advance VLSI Chip Design (Module 24513) Phase 5

Nirajan Shrestha

Aim of the Phase 5

To present complete chip layout and its results using Cadence Innovus .

Carry Select Adder (Fixed Bit)



Wallace Tree Signed Extention Multiplier after CSD Recoding

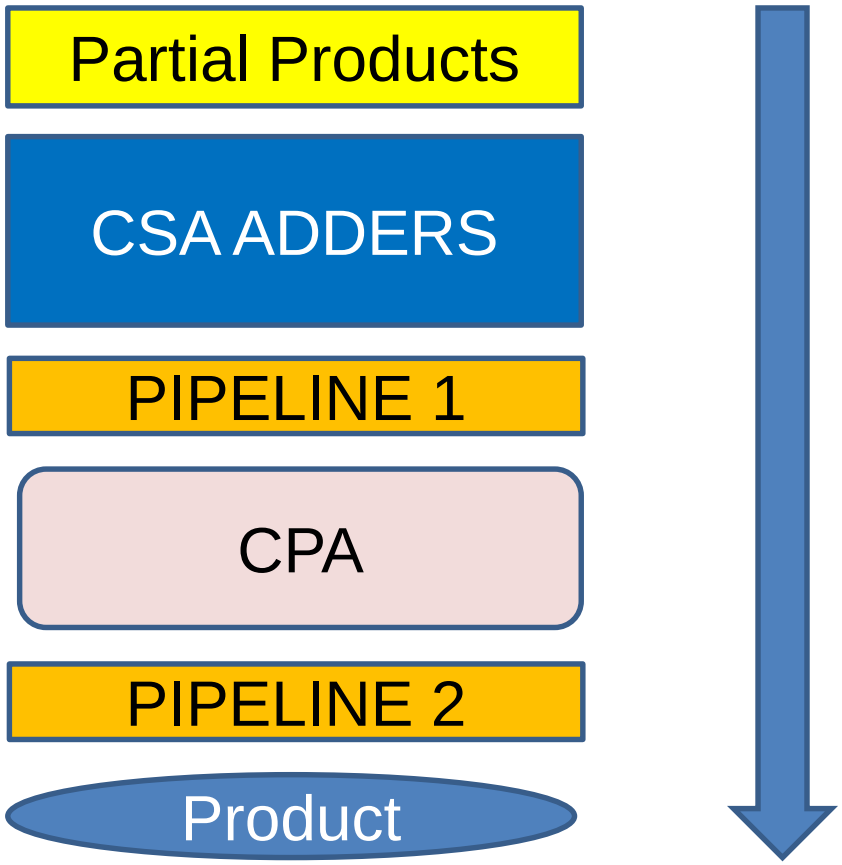
Coefficient 4,5,15,16 "1111110111111000

CSD "0000001000001000

CSD MULTIPLIER 1

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit Position
PP3	23	23	23	23	23	23	23	23	23	23	23	23	23	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				CSA 1
PP9	23	23	23	23	23	23	23	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0										
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1				
	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	5	4	3	2	1	s	0	0	0	CPA
c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c						c					

Implementing Pipeline



Final Parameters from FPGA & ASIC:

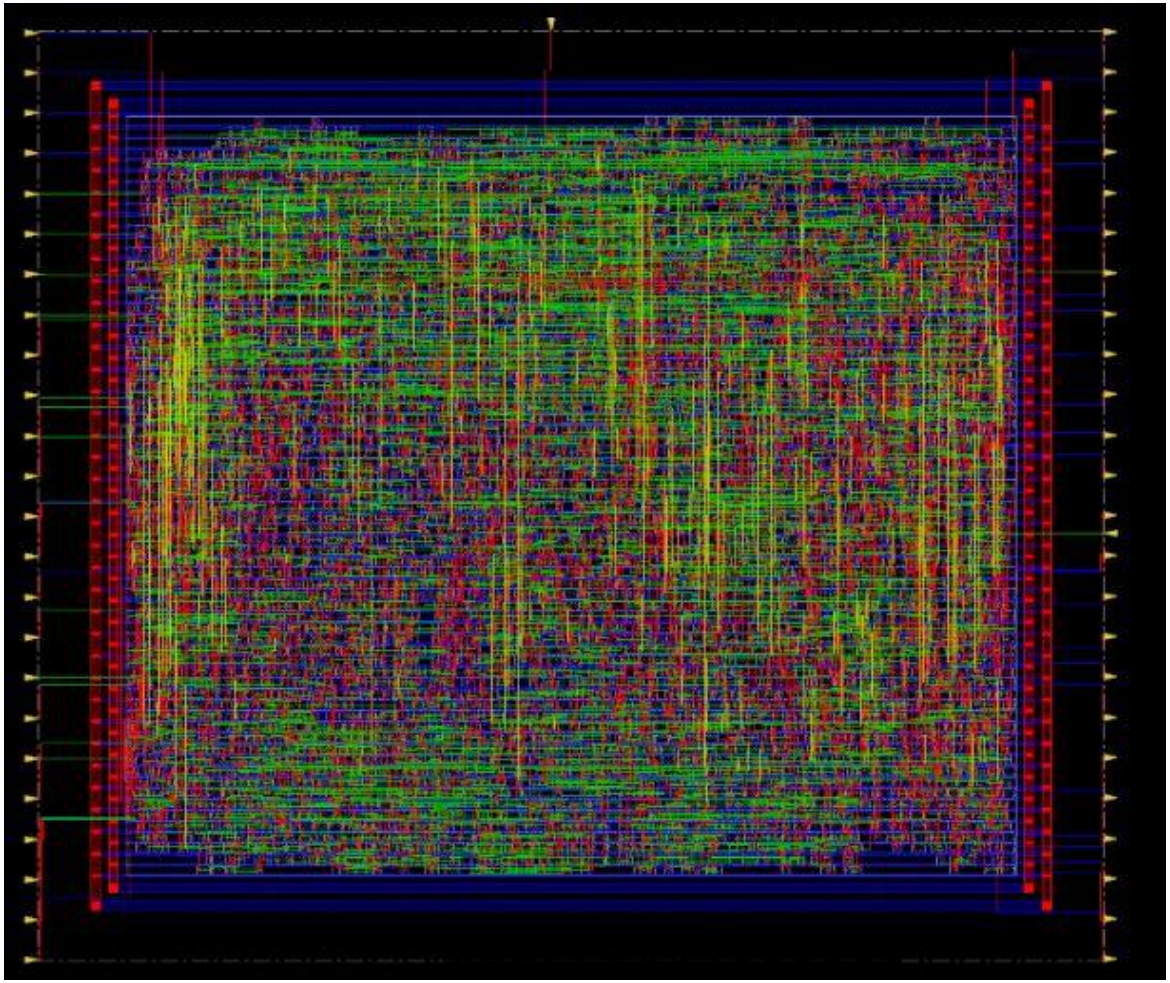
1. FPGA

	LUT	FF	WNS
	2013	~ 1400	1.998

2. ASIC

Cell Area	Total Dynamic Power	Cell Leakage Power	Operating Voltage	Frequency	Slack
26939.119520	38.3699 mW	32.1094 uW	1.2 V	1000 MHz	0.002

Chip Layout

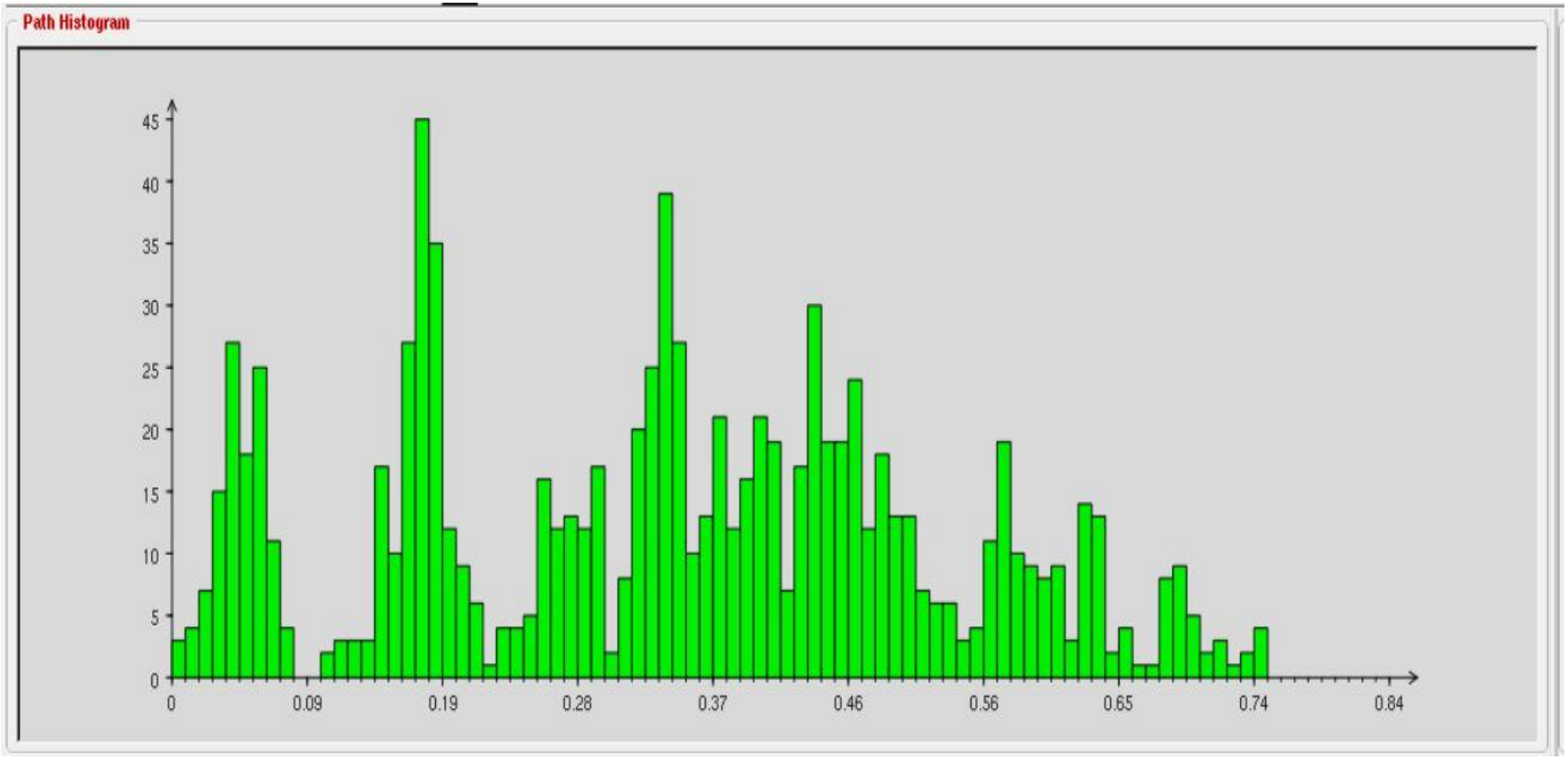


Core Utilization: 75%

Slack: 0.002

Core Margins: 20 uM

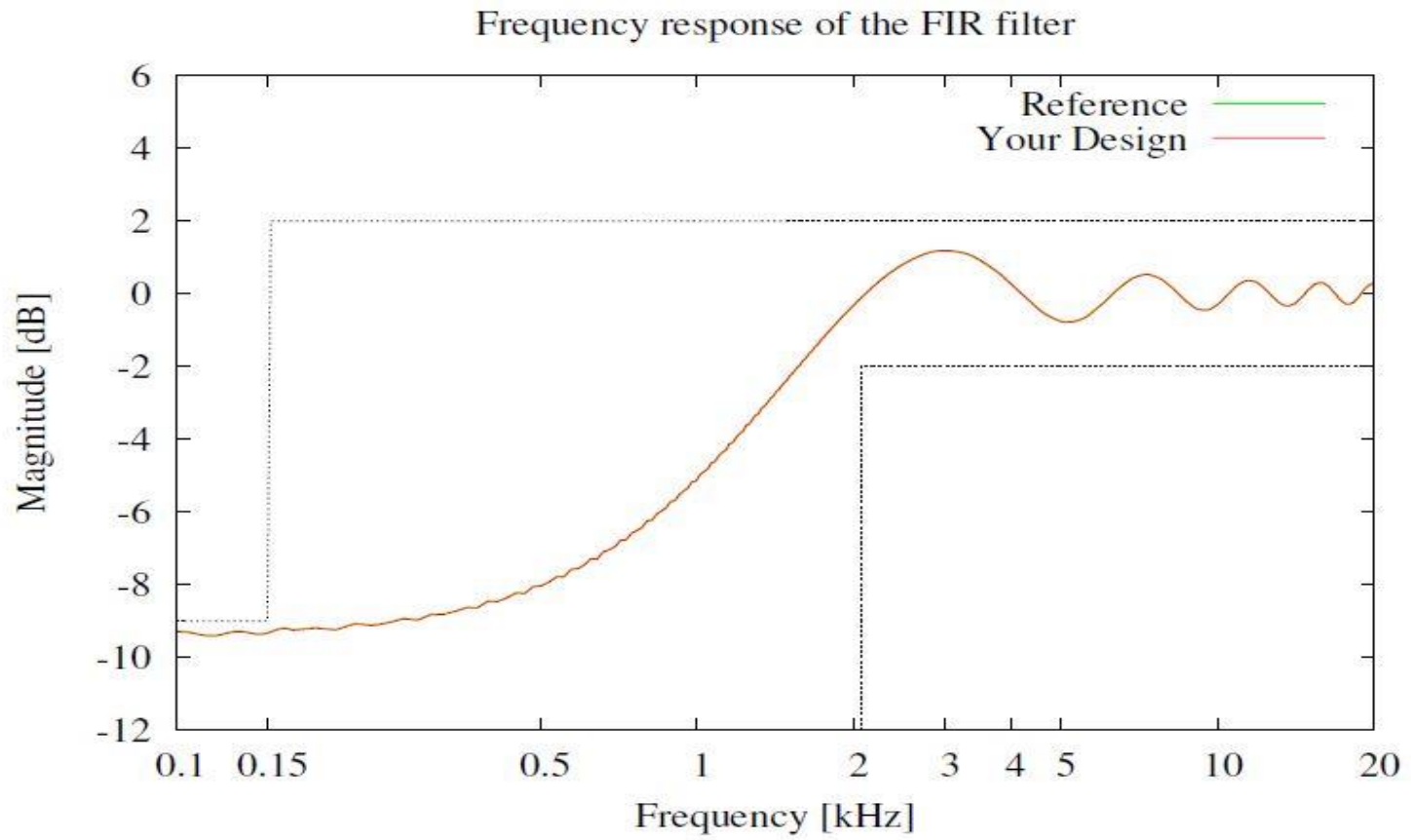
Path Histogram



Design Parameters:

Frequency Max.	1000 MHz
Power (Pdyn / p leak)	38.3699 mW / 32.1094 uW
Pipeline Stages	2
Core size	35919.468 um (2)
Core utilization	75%
Chip Size	52704.268 um (2)
Attenuation	9.193380

Frequency Response



THANK YOU

Questions!