Selected Topics in VLSI Design (Module 24513)

course and contest

results of phase 5
Presentation of complete chip layout and its results.

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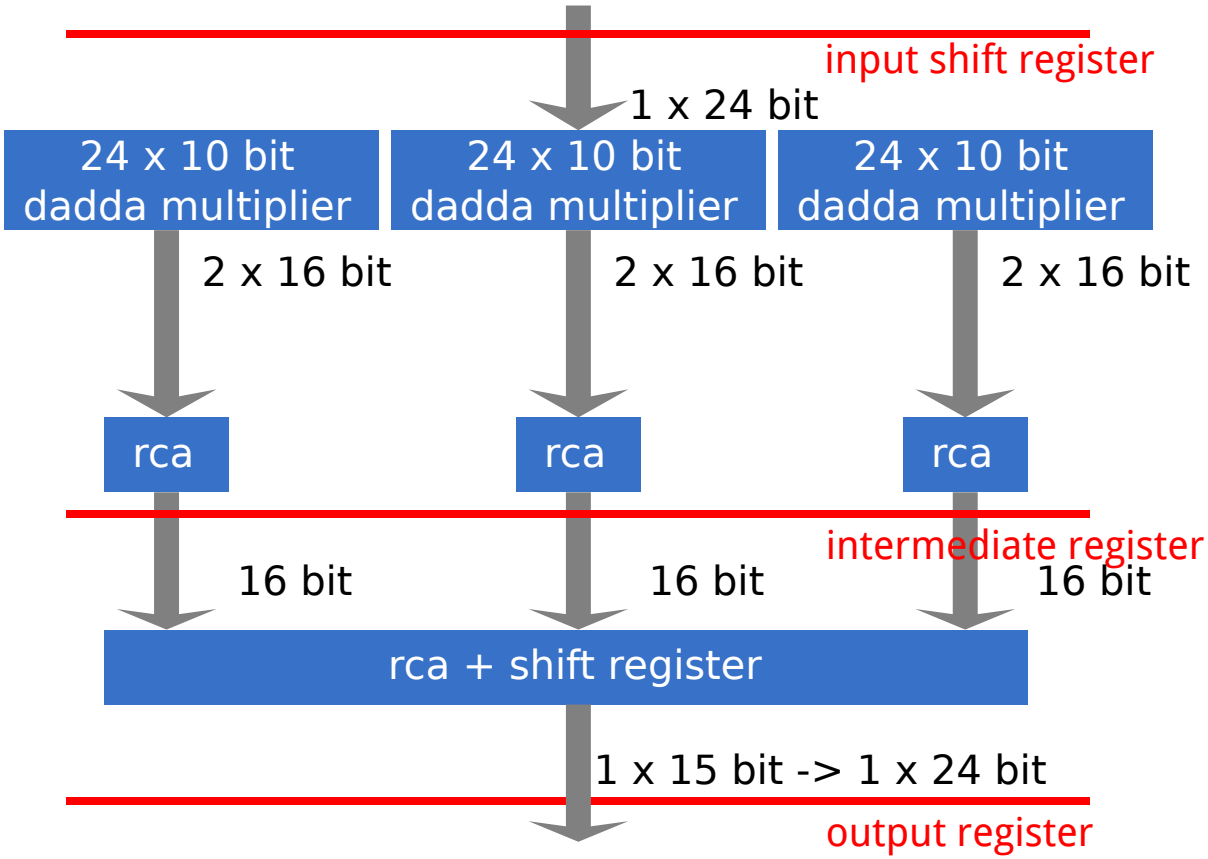
1.3 V synposys

frequency f	1 GHz
# pipeline stages	3
attenuation	-11.298298
$\mathrm{P_{dyn}}$	13.6535 mW
$\mathrm{P_{leak}}$	119.8541 nW
metric	$6.90 \times 10^9\,\mathrm{W}^{-2}$

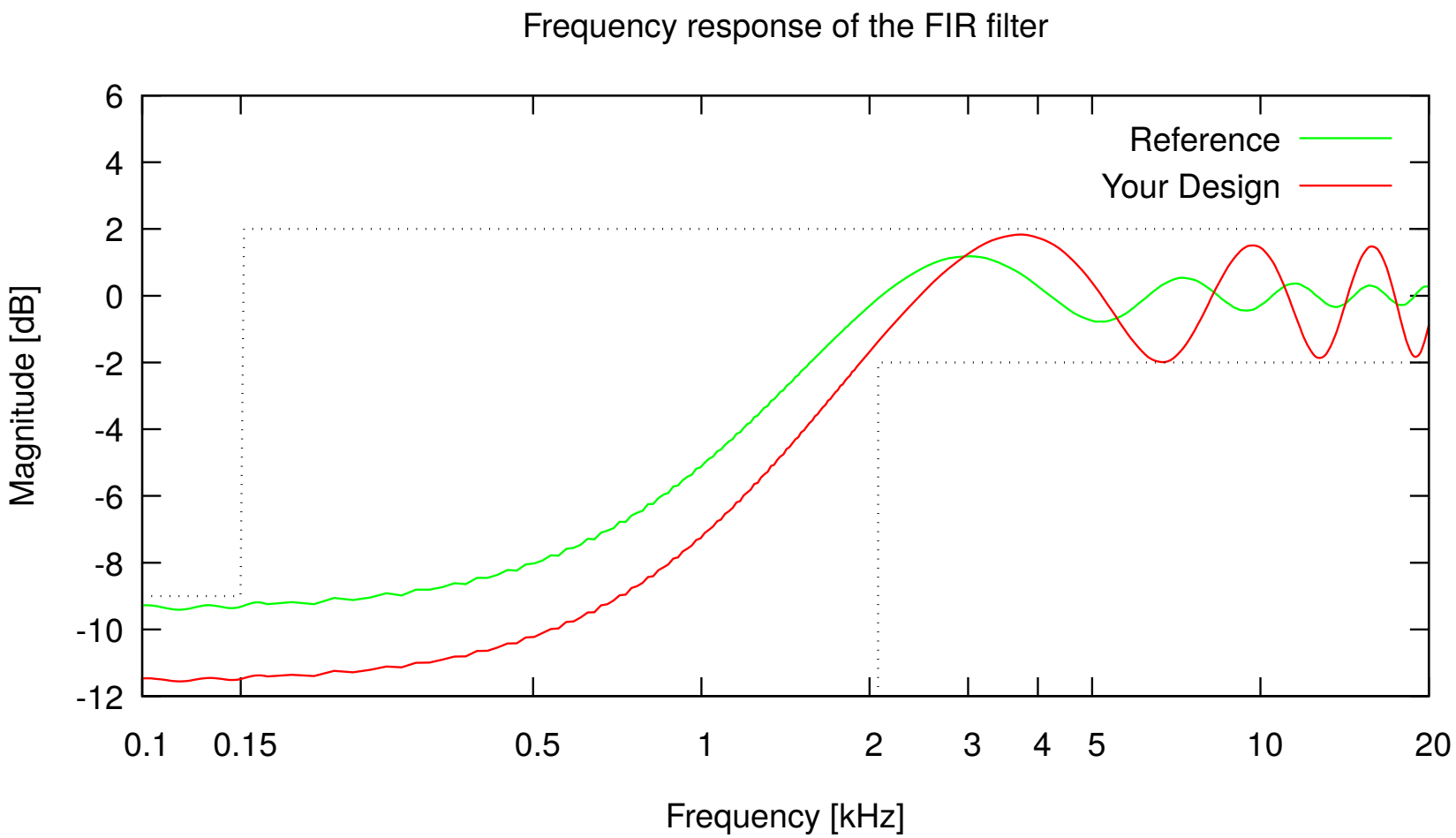
Introductory Considerations

- reduce size to lower power consumption
- wires are not for free on real chips $\rightarrow$ higher P_{dyn}

Design


input shift register
1 x 24 bit
24 x 10 bit dadda multiplier
24 x 10 bit dadda multiplier
24 x 10 bit dadda multiplier
2 x 16 bit
2 x 16 bit
2 x 16 bit
rca
rca
rca
intermediate register
16 bit
16 bit
16 bit
rca + shift register
1 x 15 bit -> 1 x 24 bit
output register

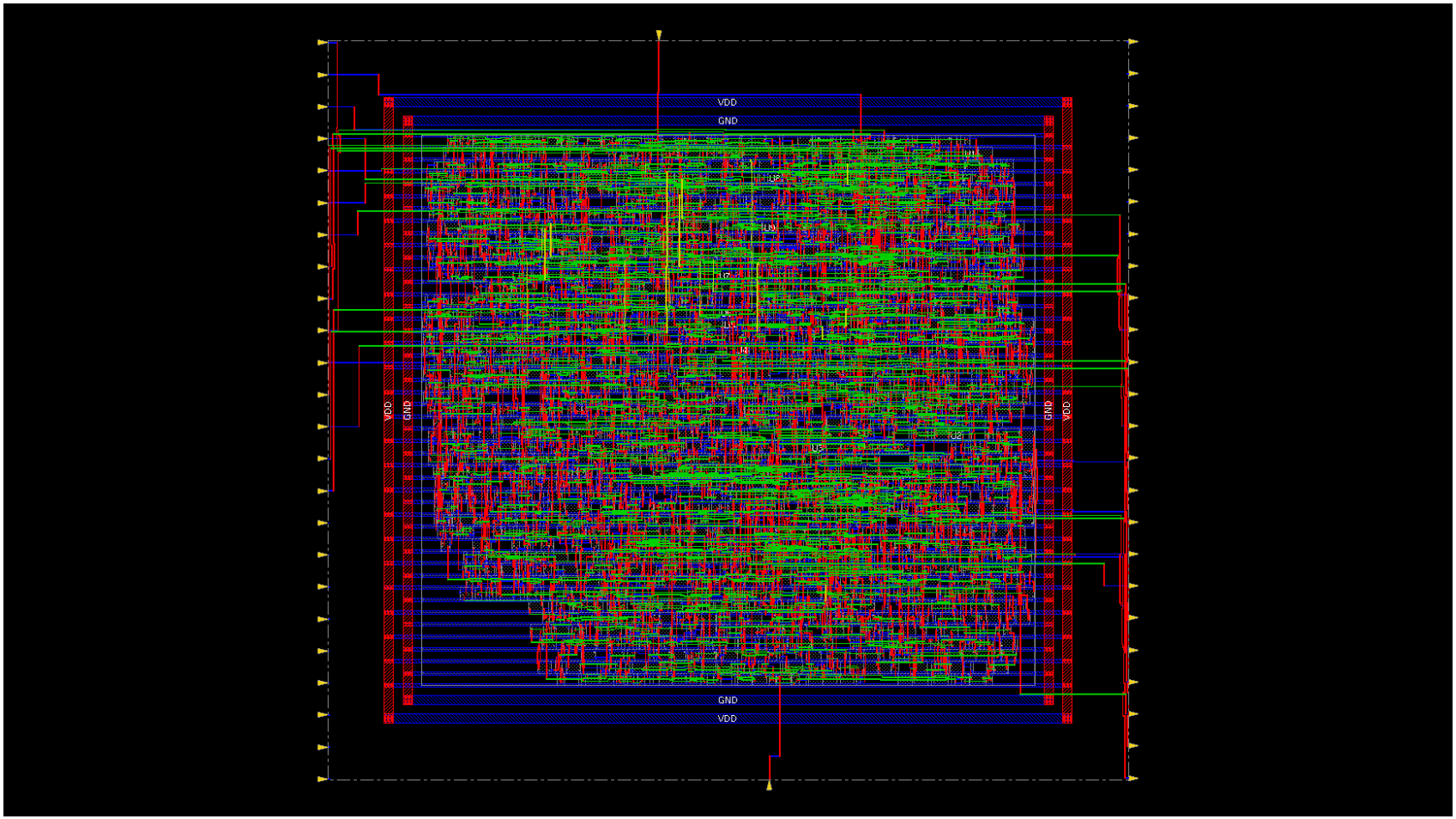
The Results


Frequency response of the FIR filter
Reference
Your Design
Magnitude [dB]
6
4
2
0
-2
-4
-6
-8
-10
-12
0.1
0.15
0.5
1
2
3
4
5
10
20
Frequency [kHz]

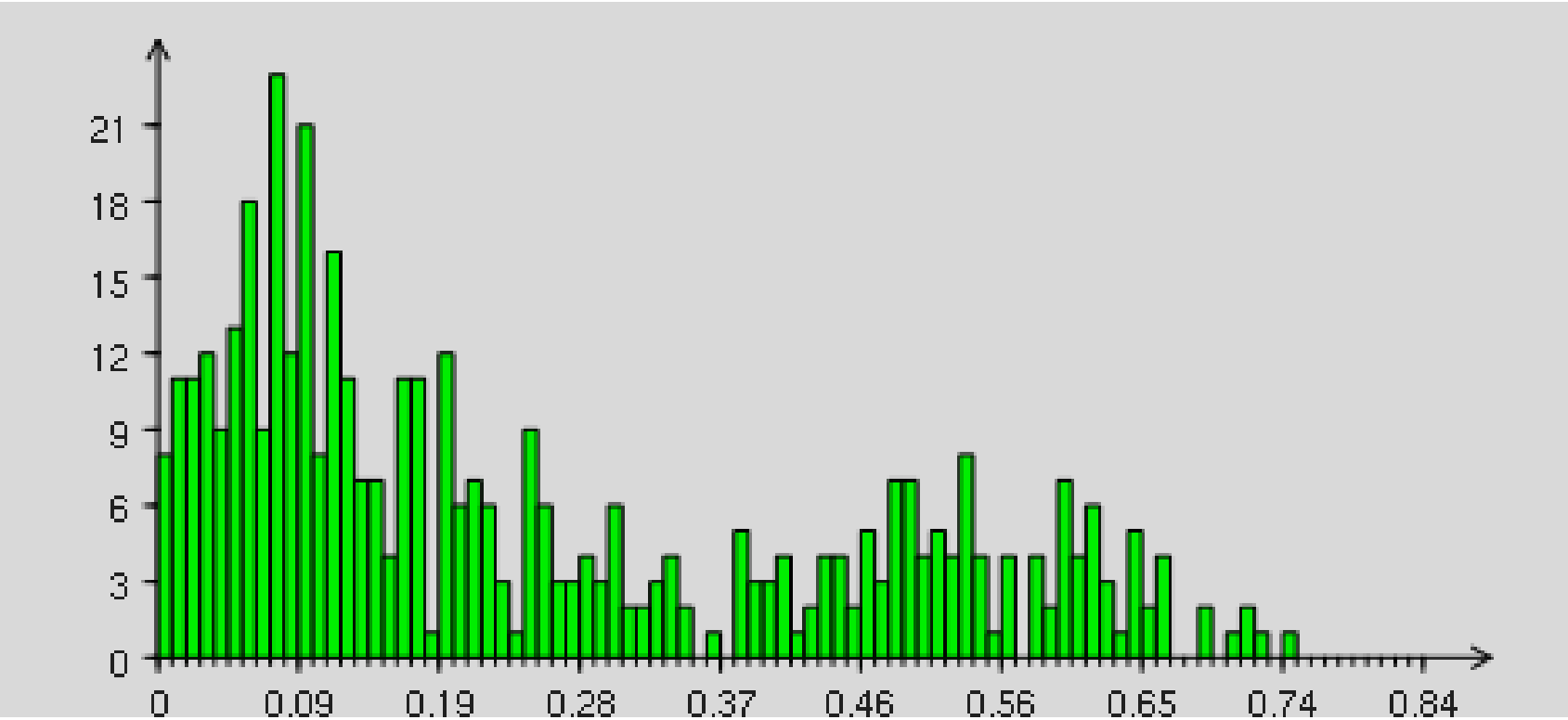
the synthesis results

timing(T_{min} / f_{max})	1 ns / 1 GHz
power (P_{dyn} / P_{leak})	14.02 mW / 119.85 nW
pipeline stages	3
benchmark	6.72×10^9 W^{-2}
core size	26 765 µm^2
core utilization	60.055 %

Core



Timing



Thank you for your attention!